Idaho[AES2550] Design Specification

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ABSTRACT

This Device Specification describes the detailed functions of the FPS19 slide sensor also known as Idaho[AES2550].

For vectors (groups of bits), ordering notation is from MSB to LSB (e.g. A2D_DATA[7:0] where bit 7 is the MSB and bit 0 is the LSB).

Numbers followed by a 'b' are shown in binary. Numbers followed by an 'h' are in hexadecimal. Hexadecimal numbers may also be shown with a 0x prefix.

When referring to the array, columns and rows are numbered starting at 0. With ball A1 in the upper left corner, column 0 refers to the leftmost column and column 191 refers to the rightmost column. Row 0 is the row at the top of the sensor and row 7 is the bottom row.

GLOSSARY

ASIC	*Application Specific Integrated Circuit.*
ATPG	*Automatic Test Program Generation.*
BIT	*Built-in Test.*
Kbps	*Kilobits per second.*
LSB	*Least Significant Bit.*
Mbps	*Megabits per second.*
MSB	*Most Significant Bit.*
Rx	*Receive.*
TBD	*To Be Determined.* The parameter under discussion is not yet finalized.
Tx	*Transmit.*
HGC	*Hardware Gain Control*

CHANGE LOG

Rev	Author	Change
0.0	sbrandt	Initial spec from latest FPS19 spec.
0.01	Sbrandt	Modified pinout table
0.02	Sbrandt	Added errata for LPO coarse setting and updated register documentation, including signals connected to the test multiplexer. Also included Appendix C as a link to the internals documentation
0.03	Sbrandt	Revised pad numbers in pinout table to reflect physical layout
0.04	Sbrandt	Added B5 as floating ball to packaging document on pg. 13
0.05	Sbrandt	Added details of USB Reset effect on patch enable internal signals
0.06	Sbrandt	Added documentation for new control bits in register 0xBF for RSR control
0.07	Sbrandt	Correct I/O table to match 2810 – cut and paste error correction
0.08	Sbrandt	Correct documentation for register test bits in 0xA2 and 0xB1
0.09	Sbrandt	Added debug message documentation for register 0xDD
0.10	Sbrandt	Additional data and warnings added to register 0xCF description. Heartbeat documentation added.
0.11	Sbrandt	Added pullup/pulldown comment in pinout section
0.12	Sbrandt	Modified absolute maximum supply values to be consistent with TSMC reliability limits

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FPS17/AES2810 Compatibility

The Idaho sensor is completely register compatible with the 2810-A2 sensor in relation to non-security functionality. The Product ID/Device ID in the USB configuration space will be unique in order to comply with USB certification requirements. The 2-byte USB Product ID will be 0x2550. The two-byte USB Device ID will by 0x19{MaskRev – 1 byte}. The 2810-A3 sensor has the added capability to reset the input buffer control when a USB RESET event occurs which is not included in the AES2550.

Overview

The document is the Design Specification for the Idaho[AES2550] fingerprint sensor. In Silicon Engineering it is referred to as FPS19.

The sensor is required to implement on-chip gain control. All on-chip gain control functions will be implemented by microcode for a custom embedded processor (the Gnat). This allows on-chip gain control improvements or bug fixes by using the microcode patching capability.

The Idaho[AES2550] sensor implements a high level command interface that allows sensor operations to be performed without having to handle all the detailed register settings necessary to perform the operation.

The sensor provides an interface to an optional external serial. The sensor provides read and write access to the flash interface with the logical operations managed by the host.

The Idaho[AES2550] sensor includes Redundant Slice Removal (RSR). RSR analyzes only the E-field data to detect motion. When RSR is disabled the sensor sends every E-field slice

When Leading RSR is enabled the sensor discards E-field slices until motion is detected. Once any motion is detected all subsequent slices are sent. If Bussed Pixel data is enabled it will be collected every slice. A Bussed Pixel Data message will be sent when a table is complete.

When Simple RSR is enabled the sensor discards E-field slices whenever there is no motion detected relative to the last slice sent. Bussed Pixel data will be collected and sent using the same criteria as for Leading RSR.

When Super RSR is enabled the sensor discards E-field slices until motion of 4 (for fast moving fingers), 5, or 6 pixels is detected between the current slice and the last slice sent. Bussed Pixel data will be collected and sent using the same criteria as for Leading RSR.

Implementing system integrity checks requires that Super RSR be enabled.

A 8K Internal Buffer provides output message storage and allows maintaining image acquisition through periods of increased system latency

When data is present in the internal buffer it is made available to the selected interface. When the USB Interface is selected, the sensor will return that data in response to a BULK IN request as soon as one of the 64 byte ping-pong buffers in the USB Interface is full. A short packet can be sent once for every frame or once for every finger with the

selection controlled by FLUSH PER FRAME in REG85. When the async serial interface is selected it will start transmitting data (if RTR is high) as soon as the first byte of data is in the internal buffer.

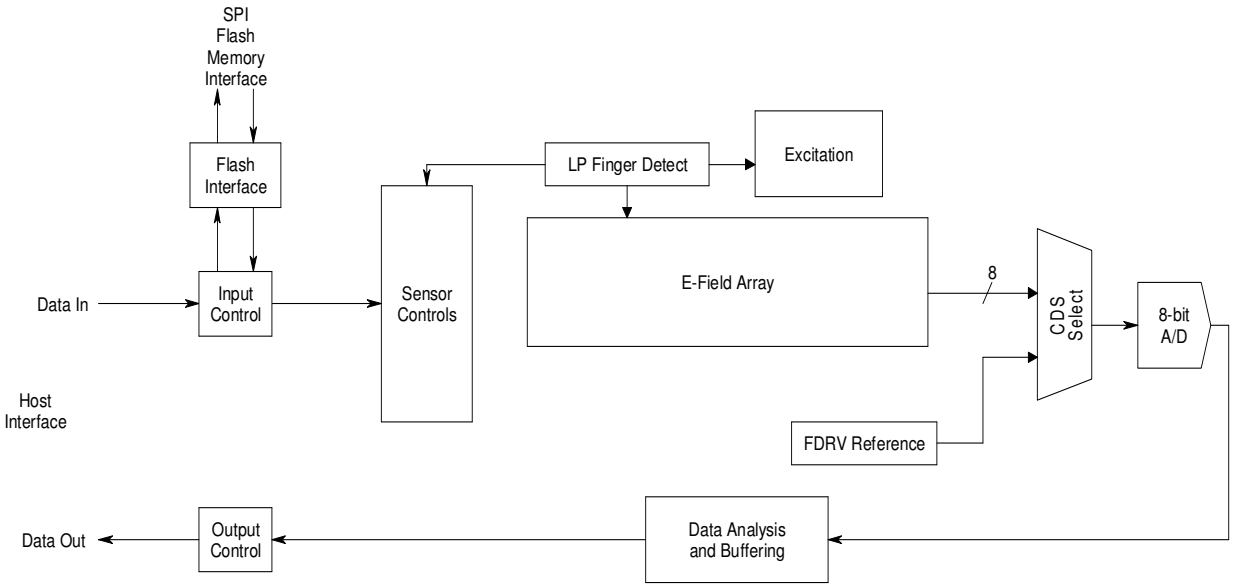
Errata

This section documents deficiencies identified in the Idaho[AES2550] sensor.

Rev	Description
A0	When LPO_CA, Register 0xB2 is set to 2 the NextMilliSecCntr is not updated correctly and the MilliSecPulse occurs every other LPO clock (400 us) instead of every ms. The bug is in logic that modifies the counter value when LPO_CA changes, suspend_resume.v. Currently LPO_CA is always set to 1 (20 KHz) during Suspend and should not change so there should be no impact from this.

Sensor Block Diagram

A functional block diagram for the sensor is shown in the figure below.



Data can be obtained from the E-field array (8x192) using individual pixels as well as an interleaved bussed pixel mode. The data is used to drive on-chip gain control functions and can be returned to the host in different formats (binary, 4-bit, 8-bit) and after being optionally filtered by algorithms designed to reduce redundant data (RSR).

The selected data is sent back to the host encrypted. Initial silicon with debug mode enabled will allow unencrypted imaging.

Sensor Pin Descriptions

Sensor pin descriptions are shown in the table below. All input pins except RESET_N [Ball B3] are required to have pull-up or pull-down devices to prevent floating input conditions.

The ball connection is defined by the AES2810 substrate – the Idaho/AES2550 must be pin-for-pin compatible with the AES2810.

Pads 1 through 22 are located on the left side of the die while pads 23 through 44 are located on the right side of the die. Pin definitions and signaling levels are shown in the table below. The two FINGERRING pins (T and B) connect to the package bezel. This requires package pins but not bond pads on the die. The Unconnected balls will be daisy-chained together [connect to tstgroup] on the package substrate to allow a simple test to determine if the balls have been attached to the substrate, even though they do not connect to the die.

Pad/Ball	Type	Pin Name	Comments	Pad Type	Level
/A1	N/A	FINGERRINGT	To Integrated Bezel	none	N/A
1/A5	Analog	VDDA2	1.8V analog power	SPVDD	1.8
2/A2	Analog	ANALOG_TST	ESD to VDDA2	ANALOG I/O	1.8
3/A6, A7	Analog	VSSA2	analog ground	SPGND	GND
4/A3	Digital	VDD2_CORE	1.8V digital core	PVDD1DGZ	1.8
5/A4	Digital	XTALIN	ESD to VDD_CORE	ANALOG I/O	1.8
6/B6	Digital	XTALOUT	ESD to VDD_CORE	ANALOG I/O	1.8
7/B3	Digital	RESET_N	ESD to VDD_CORE	ANALOG I/O	1.8
		Unconnected	floating - connect to tstgroup		
8/B1	Digital	GND_CORE	digital core ground	PVSS1DGZ	GND
9/B4	Digital	VDD2_IO	3.3 I/O Power	PVDD2DGZ	3.3
10/C6	Digital	TEST_MODE	ESD to VDD2_IO	PDIDGZ IN	3.3
11/C5	Digital	IO_SEL	ESD to VDD2_IO	PDIDGZ IN	3.3
12/C4	Digital	CLK_SEL0	ESD to VDD2_IO	PDIDGZ IN	3.3
13/C3	Digital	CLK_SEL1	ESD to VDD2_IO	PDIDGZ IN	3.3
28/C1	Digital	SIO_10	ESD to VDD2_IO	PRB08SDGZ	3.3
32/D6	Digital	SIO_9	ESD to VDD2_IO	PRB08SDGZ	3.3
31/D5	Digital	SIO_8	ESD to VDD2_IO	PRB08SDGZ	3.3
30/D4	Digital	SIO_5	ESD to VDD2_IO	PRB08SDGZ	3.3
29/D3	Digital	SIO_3	ESD to VDD1_IO/GND1_IO	PRB08SDGZ	3.3
14/D2	Digital	GND2_IO	I/O ground	PVSS2DGZ	GND
15/D7	Analog	VDD_EXCITE	3.3V Power	SPVDD	3.3
16/D8	Analog	FDRV	ESD V2XOUT/GND2_IO	ANALOG OUT	3.3
/D1	N/A	FINGERRINGB	To Integrated Bezel	none	N/A

Pad	Type	Pin Name	Comments	Pad Type	Level
23/A5	Analog	VDDA1	1.8V analog power	SPVDD	1.8
24/A6, A7	Analog	VSSA1	analog ground	SPGND	GND
25/A12	Digital	SIO_7	ESD to VDD1_IO/GND1_IO	PRB08SDGZ	3.3
26/A11	Digital	SIO_6	ESD to VDD1_IO/GND1_IO	PRB08SDGZ	3.3
27/A10	Digital	SIO_4	ESD to VDD1_IO/GND1_IO	PRB08SDGZ	3.3
28/A9	Digital	SIO_2	ESD to VDD1_IO/GND1_IO	PRB08SDGZ	3.3
29/A8	Digital	VDD1_IO	3.3V I/O Power	PVDD2DGZ	3.3
30/B7	Digital	SIO_1	ESD to VDD1_IO/GND1_IO	PRB08SDGZ	3.3
31/B12	Digital	SIO_0	ESD to VDD1_IO/GND1_IO	PRB08SDGZ	3.3
32/B8	Digital	GND1_IO	I/O gound	PVSS2DGZ	GND
33/B9	Digital	VDD1_CORE	1.8V digital core	PVDD1DGZ	1.8
34/B11		Unconnected	floating - connect to tstgroup		
35/B10		Unconnected	floating - connect to tstgroup		
36/C10		Unconnected	floating - connect to tstgroup		
37/C9		Unconnected	floating - connect to tstgroup		
38/C8		Unconnected	floating - connect to tstgroup		
39/C12		Unconnected	floating - connect to tstgroup		
40/C7		Unconnected	floating - connect to tstgroup		
41/D9		Unconnected	floating - connect to tstgroup		
42/D10		Unconnected	floating - connect to tstgroup		
43/D11		Unconnected	floating - connect to tstgroup		
44/D12		Unconnected	floating - connect to tstgroup		

Absolute Maximum Ratings

Absolute maximum ratings for power and signal pins are shown in the table below. Exceeding these ratings can result in significant loss of device reliability or can cause damage to the sensor.

Symbol	Parameter	Min	Max	Units
V_{DDIO}	I/O Supply Voltage (VDD1_IO, VDD2_IO, VDD_EXCITE)	-0.5	3.63	V
V_{DDCORE}	Core Supply Voltage (VDDA1, VDDA2, VDD1_CORE, VDD2_CORE)	-0.5	2.1	V
V_I	Input Voltage	-0.5	V_{DD}+0.5	V
V_O	Output Voltage	-0.5	V_{DD}+0.5	V
I_{IK}	Input Clamp Current VI<VSS or VI>VDD	-20	20	mA
I_{OK}	Output Clamp Current VO<VSS or VO>VDD	-20	20	mA
T_S	Storage Temperature	-65	150	C
Latch-Up	Latch-Up Immunity JEDEC 78 Class 1	-100	100	mA
ESD_{pin}	Pin-level ESD Immunity JESD22 Method A114-B	-2	2	KV
$ESD_{package}$	Package-level ESD Immunity IEC61000-4-2 Level 4 Air Discharge using AuthenTec approved reference design	-15	15	KV
T_{SOL}	Maximum Soldering Temperature (MSL=3)		260	C

Recommended Operating Conditions

Recommended operating conditions for power and signal pins are shown in the table below. These conditions are necessary for proper device operation.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDIO}	I/O Supply Voltage (VDD1_IO, VDD2_IO, VDD_EXCITE)	3.0	3.3	3.6	V
V_{DDIOAC}	I/O Supply Voltage Peak to Peak Ripple (VDD1_IO, VDD2_IO, VDD_EXCITE)			100	mV
V_{DDCORE}	Core Supply Voltage (VDD1_CORE, VDD2_CORE, VDDA1, VDDA2)	1.62	1.8	1.98	V
$V_{DDCOREAC}$	Core Supply Voltage Peak to Peak Ripple (VDD1_CORE, VDD2_CORE, VDDA1, VDDA2)			50	mV
V_I	Input Voltage	0		VDD	V
V_O	Output Voltage	0		VDD	V
V_{IL}	Low Level Input Voltage			0.3*VDD	V
V_{IH}	High Level Input Voltage	0.7*VDD			V
t_t	Digital Input Transition Time (rise, fall)	3		10	nS
T_A	Ambient operating temperature	0		70	C

DC Characteristics

DC Characteristics at recommended operating conditions are shown in the table below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage	I_{OL}=-2mA			0.3	V
V_{OH}	High Level Output Voltage	I_{OH}=2mA	VDD-0.3			V
V_{IL}	Low Level Input Current	$V_I=V_{ILmin}$	-1		1	uA
V_{IH}	High Level Input Current	$V_I=V_{IHmax}$	-1		1	uA
V_{OZ}	High Impedence Leakage Current		-1		1	uA

Operating Current

Operating currents are measured at nominal supply voltages using standard AuthenTec software and drivers.

Symbol	Parameter	Min	Typ	Max	Units
$I_{SUSPEND}$	Suspend Mode Current (C3 State)			400	uA
I_{IDLE}	Idle Mode Current		2.0		mA
I_{FD}	Finger Detect Current		2.5		mA
I_{NAV}	Navigation Current		4.5		mA
I_{IMG20}	Imaging Current, 20 cm/s		35		mA
I_{IMG30}	Imaging Current, 30 cm/s		40		mA
I_{PEAK}	Peak Current			80	mA

Interfaces

The Idaho[AES2550] sensor includes a USB 2.0 compatible Full Speed (12 Mbps) interface and an asynchronous serial interface. The interface selection is controlled by the IO_SEL with the pin assignments shown in the table below. All I/O signaling levels are 3.3V.

SIO	USB IO_SEL=0b		Async Serial IO_SEL=1b	
0	DPLUS	I/O	RXD	I
1	DMINUS	I/O	RTR	I
2	VTERM	O	TXD	O
3	SF_CS_N	O	AUTOBAUD_EN	I
4	SF_CLK	O	BAUD_SEL[2]	I
5	SF_WP_N	O	BAUD_SEL[1]	I
6	SF_MOSI	O	BAUD_SEL[0]	I
7	SF_SOMI	I	SLEEP_N	I
8	GPIO[0]	I/O	GPIO[0]	I/O
9	GPIO[1]	I/O	GPIO[1]	I/O
10	GPIO[2]	I/O	GPIO[2]	I/O

For the GPIO pins to be usable as input pins the sensor must not drive the pins at initial power up. This requires that the reset state of the pins be inputs.

Clock Select Control

The sensor includes a two-pin xtal oscillator along with an analog PLL with integrated charge pump filter components. The PLL multiplier ratio is controlled by the CLK_SEL[1:0] pins. The table below shows available options.

CLK_SEL [1:0]	PLL Multiplier	Min Fin	Nominal Fin	Max Fin
00	X8	5.435 MHz	6 MHz	6.565 MHz
01	X4	10.87 MHz	12 MHz	13.13 MHz
10	X2	21.74 MHz	24 MHz	26.26 MHz
11	X1	43.48 MHz	48 MHz	52.52 MHz

Table 1 CLK_SEL[2:0] Decode

All frequencies shown in this manual for register settings and interface timing specifications assume a 48 MHz internal clock (e.g. 12 MHz external clock and x4 PLL). **When operating with an internal clock that is at a frequency other than 48 MHz, frequencies and timing will be different than that specified in this manual.**

The sensor can operate with an internal clock that is within the range 44-52 MHz with a tolerance of 1% or less (absolute minimum = 43.48 MHz, absolute maximum = 52.52 MHz). The maximum clock frequency is guaranteed by design over all operating conditions. Exceeding this clock frequency may result in indeterminate sensor operation. The minimum clock frequency was selected to provide a symmetrical tolerance with respect to the nominal clock value. The Idaho[AES2550] sensor does not contain any dynamic logic so the sensor will continue to operate correctly at lower clock frequencies, however biometric performance may be adversely affected.

When the Async Serial interface is selected using fixed baud rates, the clock frequency must be within 2% of the nominal frequency for proper interface operation.

When the USB interface is selected the clock frequency must be within 0.25% of the nominal frequency for proper interface operation.

USB Interface

Appendix B shows the descriptor tables associated with the USB Interface. The USB interface is based on the 'inSilicon' [now Synopsys] synthesizable USB core, which is compliant with version 2.0 of the USB specification and operates only in Full Speed mode. The Idaho[AES2550] sensor is a USB low power device and provides 3 endpoints in one interface (endpoint 0, 1, and 2). Endpoint 0 supports control read and write transactions, including String Descriptor support for the device identification function in Windows. Endpoint 1 is a BULKIN endpoint for data going from the Sensor to the Host and has two 64-byte buffers operated in a ping-pong fashion. Endpoint 2 is a BULKOUT endpoint for Sensor commands from the Host.

The Idaho[AES2550] sensor supports remote wakeup and can be configured to wake the host when a finger is detected. The sensor can also be configured to begin imaging after a finger is detected and the large internal buffer allows fingerprint data to be collected while the host is waking up.

The Idaho[AES2550] sensor will detect a USB Reset condition in ~ 42.6 us (512 12 MHz clocks). A USB Reset state will generate a Master Reset to the sensor logic.

The 1.5K ohm pullup resistor used to allow device detection when using the USB interface should be connected between the VTERM pin and DPLUS. This allows the sensor to delay device connection after power up until the sensor has completed power up processing (device calibration).

The USB Transceiver re-clocks DPLUS, DMINUS, and USB_OE_N to eliminate skew between the signals caused by path delays. As an experiment to try to improve the D+/D- crossover voltage, the Idaho[AES2550] sensor will disable the 1.5K pullup resistor when the sensor is transmitting. This allows the bus loads on D+ and D- to be symmetrical. The feature can be disabled by setting REGA2[7].

The USB Interface is configured to only send a short packet when imaging is complete (the last packet sent after the finger is off the sensor). Experimental data suggests that the sensor can achieve a faster frame rate with this configuration. The sensor can be configured to send a short packet every frame by setting REG85[7].

External Serial Flash Interface

When the USB Interface is selected pins are defined to interface with an external serial flash. The sensor is the master for the interface and provides an active low chip select (SF_CS_N), a 12 MHz gated clock (SF_CLK), an active low write protect (SF_WP_N), and a data output (SF_MOSI). The sensor receives a single data pin from the external flash (SF_SOMI). The pin should have a pulldown resistor so that the sensor reads 0x00 if the serial flash does not respond.

Async Serial

The table below shows baud rate selections when AUTOBAUD_EN is low.

BAUD_SEL[2:0]	BAUD RATE
000b	115.2 Kbps
001b	230.4 Kbps
010b	460.8 Kbps
011b	921.6 Kbps
100b	750 Kbps
101b	1.5 Mbps
110b	3.0 Mbps
111b	6.0 Mbps

When AUTOBAUD_EN is high the sensor determines the baud rate by timing the first character received (0x0F). After being reset by the RESET_N pin, the sensor sends a break character (TXD low for longer than a character time). The time TXD is low is controlled by the BAUD_SEL pins. They should be set such that the receiver interprets the TXD low event as a break character. The table below shows TXD low duration vs. BAUD_SEL setting. After the break character, the sensor listens on RXD and expects the first character received to be 0x0F. By measuring the time for the four consecutive zeros and four consecutive ones the sensor establishes the bit time to be used for communication.

BAUD_SEL[2:0]	TXD low time
000b	192 us
001b	96 us
010b	48 us
011b	24 us
100b	24 us
101b	12 us
110b	6 us
111b	3 us

Reference Design/System Requirements

This will document functions expected to be handled by either the reference design or the system/software.

AES2810 Compatibility

This device must be package/pin compatible with the AES2810.

Master Reset

A Master Reset is performed when the sensor receives a write to REG81 with bit D0 set. All writes to the sensor are processed by the RISC processor so that Master Reset does not occur until the RISC processes the input buffer interrupt associated with the data and writes the data to sensor registers. One consequence of this is that a Master Reset cannot be used to reset the RISC if it is stuck in a loop or for some other reason not responding to commands. A USB Reset will allow recovery from this condition [in addition to the obvious power cycling reset].

The RISC processor will always complete current command execution before processing data from the input buffer. When the action initiated by the command is complete the RISC writes any data output from that command to the Output Buffer and resumes processing commands from the Input Buffer. If the next command is a Master Reset it will be immediately processed, resetting some registers and clearing buffer data pointers.

The only way to get a deterministic response to a Master Reset command is to stop data flow from the sensor prior to sending the Master Reset and delaying the maximum command execution time (TBD us) after the command. This would guarantee that the command is processed and that no data from previous commands remains in the sensor.

USB Reset

The USB Reset is used by the host to initialize the USB Interface prior to configuration. On previous AuthenTec sensors [except for AES2810] that is the only function performed by the USB Reset.

To provide a hardware initiated reset that can be used to reset the RISC, the Borah sensor will generate a Master Reset internally in response to a USB Reset. A USB Reset will also disable any patches that were enabled. A USB Reset will not reset the command input buffer [this is supported in AES2810-A3].

I/O Drive

The drive levels required for pins is shown in the Sensor Pin Description table. Most digital pins require 3.3V I/O; RESET_N and XTALIN are two notable exceptions. The I/O cells must not be driven when the sensor is powered off to avoid damage to the I/O cell or powering the sensor through the I/O.

Interface Bandwidth Requirements

The Idaho[AES2550] sensor includes an 8K buffer in the output data path. The buffer prevents imaging stalling during periods when the host is unable to request data from the sensor but the output bandwidth needs to be high enough to transfer a frames worth of data within the programmed frame time to prevent the buffer from filling which would in turn cause image acquisition to stall.

Overcurrent Detect Circuit

No overcurrent circuit required when using Polyamide or Kapton coating.

Power Sequencing Requirements

To prevent latchup in the I/O cells the 3.3V supply must be applied before or coincident with the 1.8V supply. At initial power on this sequence must be met by the reference design.

External Serial Flash

To use the Idaho[AES2550] sensor an External Serial Flash is required. Any flash device that meets the protocol and speed requirements for the flash interface is supported by the hardware. Applications should refer to software for a list of devices supported by the software. Software must also configure the external flash to enable the Block Protect function in order for the sensor to be able to enforce write protection on the flash.

Finger Drive

The FPS19 sensor has a separate power pin (VDD_EXCITE) for the excitation circuit. The pin should be connected to a 3.3V supply.

Reset

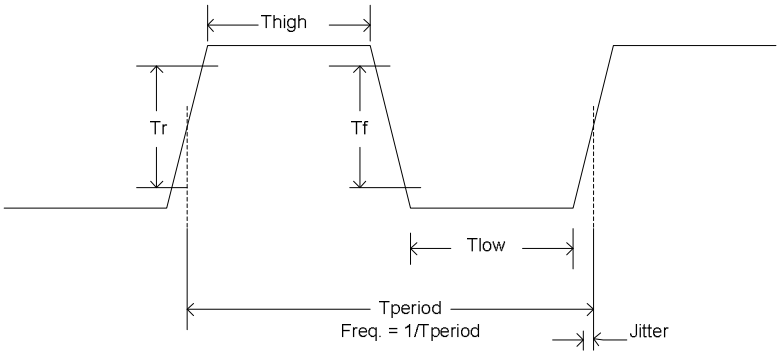
The sensor has a single active low reset pin designated RESET_N. The RESET_N pin has an internal pull-up resistor that is nominally 57K ohms but can range between 42K ohms and 72K ohms. This pin can generate a power on reset by adding a capacitor to ground.

The capacitor should be selected so that the power on reset time constant is larger than the power supply ramp time and the startup time of the oscillator. This is required to prevent clock transients as the oscillator is starting from affecting the digital logic. The oscillator startup time is expected to be less than 3 ms.

Internally the sensor delays the release of reset by 200 us nominally to allow the PLL to lock. The host should wait at least 400 us after reset is released before attempting to communicate with the sensor.

External Clock

When driving an external clock into the XTALIN device pin refer to the following timing specification.



Parameter	Minimum	Maximum
Freq.	Freq.(nominal) – 1%	Freq.(nominal) + 1%
Jitter		Tperiod*1%
Tr	-	10% of Tperiod
Tf	-	10% of Tperiod
Thigh	45%*[Tperiod]	55%*[Tperiod]
Tlow	45%*[Tperiod]	55%*[Tperiod]

Table 2 External Clock Timing Specifications

Operation

Power On Reset

Power On Reset occurs when the sensor is reset by the RESET_N pin. This pin is typically used for power on reset by adding an external capacitor to ground. The pin has an internal pull-up resistor that is nominally 57.1K, with one RC being the typical reset time. The reset time should be longer than the power supply ramp time plus the oscillator startup time so that both the PLL and the digital logic are held in a reset state until the oscillator has started. After the RESET_N pin goes high the sensor keeps clocks disabled for 200 us nominally (100 us minimum, 400 us maximum) to allow the PLL to lock. The clock blocking is skipped if the CLK_SEL pins are set to select PLL BYPASS.

After a power on reset the sensor will perform calibration. Sensor calibration includes adjusting the LPO_FA setting to obtain a LPO frequency as close to 20 KHz as possible, building a gain vs. Offset DAC table for E-field imaging, and calibrating the FD Thresh DAC used in Low Power Finger Detect. The A0 silicon includes only Offset DAC calibration in ROM.

Master Reset

A Master Reset is performed when the sensor receives a write to REG81 with bit D0 set. In the Idaho[AES2550] sensor all writes to the sensor are processed by the RISC processor so that Master Reset does not occur until the RISC processes the input buffer interrupt associated with the data and writes the data to sensor registers. One consequence of this is that a Master Reset cannot be used to reset the RISC if it is stuck in a loop or for some other reason not responding to commands.

The RISC processor will always complete current command execution before processing data from the input buffer. When the action initiated by the command is complete the RISC writes any data output from that command to the Output Buffer and resumes processing commands from the Input Buffer. If the next command is a Master Reset it will be immediately processed, resetting some registers and clearing buffer data pointers.

The only way to get a deterministic response to a Master Reset command is to stop data flow from the sensor prior to sending the Master Reset and delaying the maximum command execution time (TBD us) after the command. This would guarantee that the command is processed and that no data from previous commands remains in the sensor.

USB Reset

The USB Reset is used by the host to initialize the USB Interface prior to configuration. On current AuthenTec sensors that is the only function performed by the USB Reset.

To provide a hardware initiated reset that can be used to reset the RISC, the Idaho[AES2550] sensor will generate a Master Reset internally in response to a USB Reset.

Command Processing

Low level sensor control is available by writing to sensor registers. Register data writes always take two bytes. The first byte specifies the register address and the second byte specifies data to be written to that register. High level sensor commands are either single byte or multi byte. For multi byte messages the header is followed by two bytes that specify the number of bytes remaining in the message. The byte count is sent most significant byte first.

Sensor messages can be validated using the Challenge-Response #1 (CR1) or CR2 message signing algorithms used on current AuthenTec sensors.

Finger Detect

The sensor implements multiple methods for detecting a finger. The Finger Detect method is selected by FD SEL (REG8A). When set to 00b the sensor uses the Edge Based Finger Detect method used on ER sensors. Using fixed operating settings and a calibrated channel the sensor obtains full array images. For each image a power number is computed by summing the product of the histogram BIN value multiplied by the BIN weight (e.g. (BIN0 * 0) + (BIN1 * 1) + … + (BIN15 * 15)). When the current image power exceeds the last image power by more than the value programmed in Finger On Threshold (REG87) a finger is detected. If the LPO IN register is set to zero a single detect cycle is performed. If the LPO IN register is non-zero the sensor will perform finger detect cycles at the rate specified by LPO IN until a finger is detected.

When Edge Based Finger Detect is selected, the oscillator and PLL can be shut off if their startup time is shorter than the detect time. The oscillator and PLL are shut off only if it is allowed. When the USB interface is selected it is allowed if the sensor is in the USB Suspend state. If the Async Serial interface is selected it is allowed if SLEEP_N is low. The oscillator and PLL are re-enabled in a staggered fashion (oscillator enabled, wait Osc On Delay, PLL enabled, wait PLL On Delay) before the start of the next detect cycle since the oscillator and PLL are required to image the array.

When Low Power Finger Detect (LPFD) is selected, the sensor busses the pixel plates together and measures the sampled response with a comparator that has a programmable threshold. The LPO in register is used in the same fashion as Edge based to control detect rate. LPFD can be performed while the oscillator and PLL are off.

In Idle mode finger detect is initiated by issuing the Run FD command. If the LPO IN register is set to zero a single detect cycle is performed with the sensor returning REG83 after the command completes. If the LPO IN register is non-zero the sensor will perform finger detect cycles at the rate specified by LPO IN until a finger is detected. After a finger is detected the sensor will return REG83 address and contents. This also applies to USB; when Remote Wakeup is enabled and the device is in the USB SUSPEND state, the device will do finger detect cycles until a finger is detected, send Resume signaling to notify the host of a wakeup event, and then send REG83 address and contents to indicate a finger detect occurred.

When Imaging or Nav modes are selected the sensor will first check for a finger. If a finger was detected with a previous Run FD command in idle mode the finger detect

cycle is skipped. If the LPO IN register is set to zero, finger detects are performed as fast as possible until a finger is detected or Force Finger On is set. If the LPO IN register is non-zero the sensor will perform finger detect cycles at the rate specified by LPO IN until a finger is detected. Imaging mode continues finger detect cycles until a finger is detected and continuous or N-shot scanning is enabled.

Operating Modes

The Idaho[AES2550] sensor has three operating modes: idle, imaging, or navigation.

Idle

Some sensor commands are valid only when the sensor is in idle mode as indicated in Table 1. These include the commands that allow reading or writing an external flash device and reading or writing RISC Program RAM.

In Idle mode the sensor will check for a finger after receiving the Run Finger Detect command. If the LPO IN register is set to zero a single finger detect cycle will be performed and the sensor will return a Single Register Message for REG83. If the LPO IN register is set to a non-zero value, finger detect cycles will be performed continuously at the programmed rate. A single register message will be returned only when a finger is detected. Continuous Finger Detect can be exited by the high level Set Idle Mode command or a master reset.

Idle – Read/Write External Flash

The flash interface is available only when using the USB interface and can be used to read or write to an external flash device. The sensor provides a 5 wire interface consisting of SF_CS_N, SF_CLK, SF_WP_N, and SF_MOSI signals to the flash and a SF_SOMI signal from the flash. The reference design should include a pulldown resistor on the SOMI signal so that it is in a known state when the flash is not driving the data line.

The sensor provides two commands to access the flash: Write External Flash and Read External Flash. Each of the command allows control over the write protect signal to the flash (SF_WP_N) and the state of the chip select signal (SF_CS_N) after the command.

Reading from the flash typically requires using both the Write External Flash and Read External Flash commands. The following example shows how to use the external flash interface to read the manufacturer and device ID codes from a Winbond W25P40 4-Mbit serial flash.

The 25P40 data sheet shows the read device ID operation involves sending 0x90 to the flash followed by three bytes of 0x00. The flash responds with a 1-byte manufacturer ID followed by a 1-byte device ID code.

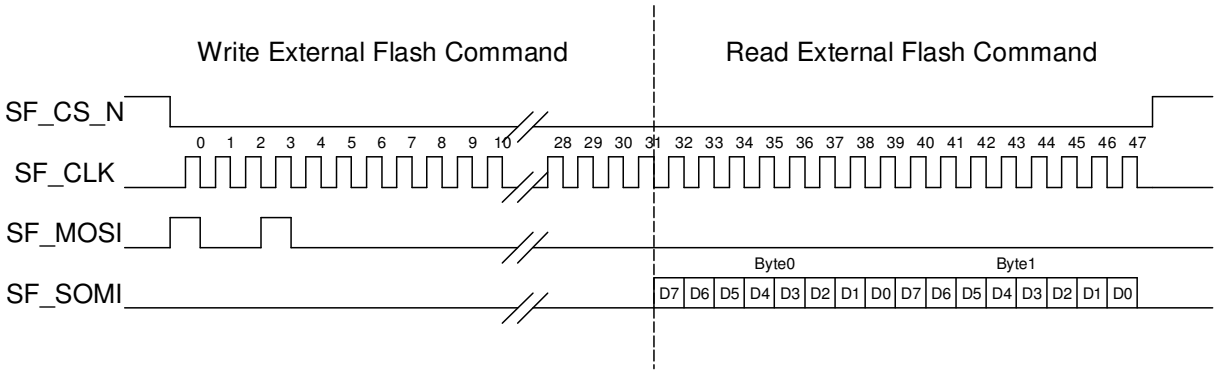
First a Write External Flash command is used. The input data for the command is shown below.

Byte	Value	Description
1	0x40	Write External Flash command
2, 3	0x0005	Number of bytes to follow
4	0x01	Control to leave SF_CS_N asserted after command
5	0x90	First byte of data to send to flash
6	0x00	
7	0x00	
8	0x00	Last byte of data to send to flash

Next a Read External Flash command is used to read 2 bytes of data from the flash. The input data for the command is shown below.

Byte	Value	Description
1	0x41	Write External Flash command
2, 3	0x0003	Number of bytes to follow
4	0x00	SF_CS_N inactive after command
5	0x00	Read 2 bytes from the flash
6	0x02	

This sequence of sensor commands results in the following controls to the external flash.



The Write External Flash Command sends 4 bytes of data to the external serial flash. Data is sent most significant bit first and changes at the falling edge of the serial clock. Chip Select is left active at the end of the command to allow the resulting data to be read using the Read External Flash command. The Read External Flash Command sends SF_CS_N and SF_CLK to the external flash and captures data on SF_SOMI. Data is captured on the rising edge of SF_CLK and is read most significant bit first. The two bytes read from the flash are assembled into an External Flash Data Message that the host can read. The message content is shown below.

Byte	Value	Description
1	0xD0	Msg Id for External Flash Data Message
2, 3	0x0002	Number of bytes to follow
4	Byte0	First byte read from flash (0xEF for Winbond W25P40)
5	Byte1	Second byte read from flash (0x12 for Winbond W25P40).

Similar combinations of Write External Flash and Read External Flash commands can be used to perform any serial flash command. From the sensors perspective the Write Serial Flash message length should be kept to < 1K byte and there is so restriction on the number of bytes that can be read using the Read External Flash command. The flash device itself may have additional restrictions.

The Write and Read External Flash commands also allow specifying the state of the write protect pin to the external flash. The state of the write protect pin is further qualified with an sensor internal register state (FLASH WRITE EN) that is set when writing to the external flash is allowed. Note that the write protect pin to the flash device only protects writing to the flash status register. The status register can be configured to provide block write control to the flash. Refer to the flash device data sheet for additional details. The host must configure the external flash to use the Block Protect bits in order for the sensor FLASH WRITE EN bit to serve any function.

Imaging

In imaging mode the sensor will acquire data from the sensor array after a finger is detected. The data acquired can optionally include Bussed Pixel measurements. Image data acquisition is initiated using the Get Enroll Image command.

Imaging starts when the Sensor Mode is set to imaging and N-shot or Cont Scan is selected. The sensor does not perform any finger detect cycles or require the presence of a finger to start imaging unless Run FD is also selected. The Get Enroll Image command sets the Run FD bit.

When imaging the analog circuits (excitation, array, and A/D) are enabled prior to imaging to allow references to startup and stabilize. The time between being enabled and the start of imaging is programmable.

The time required to sample each column of the array is dependent on the settings for *Excite Freq* and *Excite Cycle* (REG8B) and *E-field Pixel Average* (REG93). The table below shows the column scan rate using expected imaging settings (1.5 MHz excitation, sample cycle set to 1, and no averaging).

Conditions	Column Time
E-field Only	3.167 us

The Idaho[AES2550] sensor includes the capability to take bussed pixel measurements at the end of every slice. The feature is enabled by setting the Bussed Pixel En bit in REG8A. The sensor will use the measured values to populate a table indexed by frequency and phase settings. Separate tables are maintained for Reference measurements

and Array measurements. When the table is complete the sensor will send a message containing the table and start populating a new table. A table is considered complete when all entries are populated. When imaging is complete any existing uncompleted tables will also be sent. The table is initialized to 0xFF so any unpopulated entries will be 0xFF.

Image frames are acquired at the frame rate programmed in REG99 and REG9A. If the frame rate has not been programmed or has been set to zero the sensor acquires images as fast as it can. This can result in variability in the actual frame rate due to interface timing. An 8K internal buffer allows collecting some image frames at a faster rate than the interface is capable of supporting. The sensor can collect images at the programmed rate until the internal buffer is full. As image slices are collected messages are assembled in the internal buffer and data is made available to the host after a decision has been made to send the data.

The maximum slide speed assumes that the successive slices have to overlap by at least two rows. With a finger moving at the maximum slide rate each slice of data would include an E-field image with 6 unique rows. The maximum slide is calculated from

$$MaxSlideSpeed(cm/s) = \frac{30.48}{FrameRate(ms)}$$

A programmable Run-On count allows collecting images when a finger is no longer detected. This is intended to allow for the finger bouncing off the sensor during sliding.

Data is sent from the sensor in the order it is acquired. A typical message sequence is shown below.

Message	Description
1	E-field data, frame #1
2	E-field histogram, frame #1
3	E-field authentication, frame #1
4	E-field data, frame #2
5	E-field histogram, frame #2
6	E-field authentication, frame #2
|	|
M	E-field data, frame #N
M+1	E-field histogram, frame #N
M+2	E-field authentication, frame #N
M+3	Bussed pixel data #1
|	|
last	Bussed pixel data #P

Figure 1 Imaging Data Messages – RSR Disabled

For each frame E-field data is sent first followed by E-field histograms and authentication data if enabled (REG8F). If Bussed Pixel data is enabled, Bussed Pixel Tables are sent after all E-field data has been sent.

Image data collection continues for the number of frames specified by Run On after the frame where a finger was no longer detected. Finger Off detection while imaging occurs when the amount of white in the image received from the A/D (BIN0 of the histogram) exceeds the value programmed in FD Off Threshold. If imaging was initiated using the Force Finger On bit it continues until the Force Finger On bit is no longer set and Finger Off detection occurs.

If the sensor is imaging in Cont Scan mode, the N-shot count value is used as a modulo value. After finger off is detected and the number of frames specified by Run On have been acquired the sensor will continue to acquire images until the total number of frames acquired is a modulo of the N-shot setting.

After the last image frame is obtained, the sensor will stay imaging mode and start looking for a finger if Mode Auto Restart (REG80) is set. If Mode Auto Restart is not set, the sensor will return to Idle mode.

Imaging – Interleaved Impedence Mode

Imaging mode optionally can include bussed pixel and reference measurements at the end of every image frame. Impedence Mode is enabled by setting REGA2[1].

When Impedence Mode is enabled four additional measurements are made after every image frame. The measurements will include 2, 3, or 4 Bussed Pixel measurements and 0, 1, or 2 Reference measurements. The measurements sweep phase from BP Phase Init to BP Phase Stop in steps of BP Phase Step. The measurements are made at each frequency from BP Freq Start to BP Freq Stop.

Impedence Mode has a simple gain control algorithm that is used to ensure that the Bussed Pixel data is not saturated. Impedence Mode starts out using the programmed value of BP Gain. If any of the Bussed Pixel measurements are saturated (0xFF), gain is reduced by one step and the phase sweep is restarted from the last measurement point. Gain control can be disabled by selecting Fixed BP Gain.

Impedence mode includes a debug mode that allows getting impedence data every frame. Impedence debug mode is enabled by setting REGDC[3] and having Impedence Mode enabled. When enabled debug messages are returned every frame with the format shown below.

Byte	Value	Description
1	0xD9	Msg Id for debug message
2,3	0x002C	Message Length = 44 bytes
4	REF_FLG	0 = BP Data, 1 = Ref Data
5	PHASE	Phase Setting
6	GAIN_FREQ	Gain in upper nibble, Freq in lower nibble
7-14	DATA	8 bytes of measured data
15	REF_FLG	0 = BP Data, 1 = Ref Data
16	PHASE	Phase Setting
17	GAIN_FREQ	Gain in upper nibble, Freq in lower nibble
18-25	DATA	8 bytes of measured data
26	REF_FLG	0 = BP Data, 1 = Ref Data
27	PHASE	Phase Setting
28	GAIN_FREQ	Gain in upper nibble, Freq in lower nibble
29-36	DATA	8 bytes of measured data
37	REF_FLG	0 = BP Data, 1 = Ref Data
38	PHASE	Phase Setting
39	GAIN_FREQ	Gain in upper nibble, Freq in lower nibble
40-47	DATA	8 bytes of measured data

Navigation

In navigation mode the sensor takes a set of images separated by pre-programmed times. Image collection begins when a finger is detected on the sensor and stops when the finger is no longer detected. The host will correlate the set of images against one another to determine the finger's motion. The programming of the time intervals involves three settings: Time Base (T), Multiplier (M), and Repetitions (R). The Time Base value is programmed as the number of Low Power Oscillator (LPO) clocks to wait between the start of the first image of a set and the second image of a set. The Multiplier value tells the sensor how much longer to wait for subsequent packets. The Time Base is iteratively multiplied by the multiplier for each image until the number of Repetitions is reached.

The figure below illustrates the spacing of the image frames for a "nav packet" with M=2 and R=3.

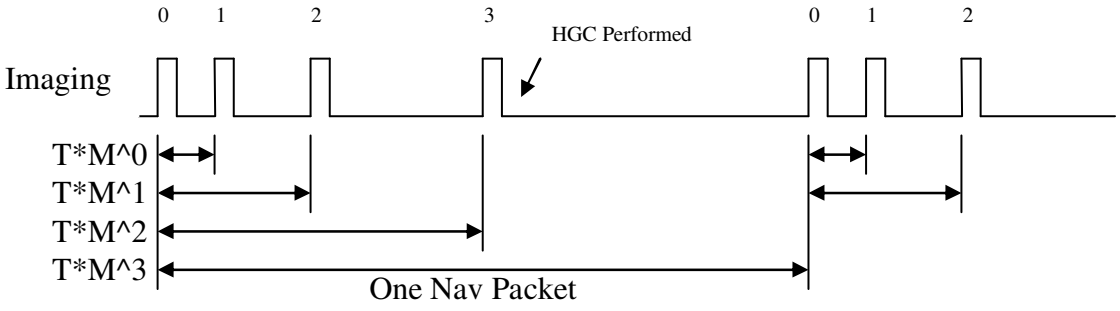


Figure 2 NAV Image Timing for M=2, R=3

In order to maintain the proper ratios between all the images within a "nav packet", the Low Power Oscillator (LPO) is used to measure all the time gaps. The LPO runs at a nominal rate of 20kHz and is calibrated to ensure that the frequency error from nominal is less than 10%.

In NAV mode the sensor always behaves just as it does in imaging, except for doing more than one frame per "packet". All the same data formatting available in imaging mode applies to NAV mode. Hardware Gain Control, if enabled, is run only after the fourth image segment in each cycle, which keeps gain settings consistent among the three image segments within the cycle. The same concept holds true for detecting when a finger was removed and the delivery of a modulo number of Nav packets in Cont Scan mode based on the N-shot count.

The single NAV "packet" contains all the frames requested by the Repeat number. The end of a packet is delimited by a short USB transfer, that is, a transfer of less than 32 data bytes. If a packet contains a multiple of 32 bytes, then the sensor will transfer a packet with zero data bytes at the end of the NAV data to delimit the packet.

Patching

The sensor architecture allows the firmware to be patched.

Patching is accomplished in two steps. First the Write Program RAM command is used to load a patch into Program RAM. The table below shows reserved areas in the Program RAM.

Address	Contents
0x2000-0x37EF	Available for patches
0x37F0-0x37FF	Reserved for program stack pointer

Table 3 Program RAM Memory Map

After the patch is written to Program RAM a patch vector is loaded using the Enable Patch message. The message specifies the vector number, program address to be re-vectored and the destination address. Up to 8 active patches are supported. A Disable Patch command is provided to turn off re-vectoring, and a Read Program RAM command can be used to verify patches.

The re-vector logic replaces a Program Memory read at the specified address with a *long* instruction and a read from the specified address + 1 with a *jump destination* instruction.

Message Formats

Data To Sensor

Single Byte Commands

The high level commands 0x00 – 0x3F are single byte commands. The RISC processor responds to the commands by configuring the sensor as necessary to perform the command. Single Byte Command Header values are shown in the table below.

Msg Id	Message Contents	Mode
0x00	Set Idle Mode	any
0x01	Run Finger Detect	Idle
0x02	Get Enroll Image	any
0x03	Get Navigation Data	any
0x04	Run BIST	Idle
0x05	Run Timer	Idle
0x06	Run Cal	Idle
0x07	Read ID	Idle
0x08	Read Registers	Idle
0x10	Read Cal Table	Idle
0xFF	Filler byte, ignored	any

Table 4 Single Byte Command Headers

The table below shows Single Byte Commands that can also be initiated by register writes.

Command	Single Byte	Equivalent Register Writes	Required Mode
Set Idle Mode	0x00	0x80, mode to 00b	any
Run Finger Detect	0x01	0x81, 0x08	Idle
Get Enroll Image	0x02	0x80, mode to 01b 0x81, 0x09	any
Get Navigation Data	0x03	0x80, mode to 10b 0x81, 0x09	any
Run BIST	0x04	0x81, 0x80	Idle
Run Timer	0x05	0x81, 0x40	Idle
Run Cal	0x06	0x81, 0x20	Idle
Read ID	0x07	0x81, 0x10	Idle
Read Reg	0x08	0x81, 0x02	Idle

When the high level commands are processed the RISC will perform the register writes needed to initiate the command. The commands Run BIST, Run Timer, Run Cal, Read ID, Run FD, and Read Reg will clear only the register bit that initiated the command upon completion. This allows multiple commands to be initiated by a single register write

or additional commands to be sent before the first command is complete. The commands are prioritized with Run BIST (initiated by bit D7) being the highest priority and Read Reg (initiated by bit D2) being the lowest priority.

Commands that are issued when the sensor mode is not set appropriately for the command will be ignored.

Multi Byte Commands

The high level commands 0x40 – 0x7F are multi-byte commands. The command is followed by a two byte field indicating the number of bytes remaining in the message. Additional bytes are included as required by the command.

Mgs Id	Message Contents	Mode
0x40	Write External Flash	Idle
0x41	Read External Flash	Idle
0x42	Write RISC Program RAM	Idle
0x43	Read RISC Program RAM	Idle
0x5A	Enable Patch	Idle
0x5B	Disable Patch	Idle
0x5C	Load Offset Cal Table	Idle
0x5D-F	0x5D thru 0x5F Unused	
0x65	ReservedCommandA	Idle
0x66	ReservedCommandB	Idle
0x80-0xDF	Precedes Register Data	any

Table 5 Multi Byte Command Headers

Write External Flash

The Write External Flash message is used to write to an external flash device. This command is valid only when the sensor is in idle mode and the USB interface is selected. The Write External Flash message is shown in Figure 3.

Byte	Value	Description
1	0x40	Write External Flash command
2	LEN_H	Upper byte of number of bytes to follow
3	LEN_L	Lower byte of number of bytes to follow
4	CTRL	Control for SF_WP and SF_CS_N [SF_WP = serial flash write protect and blocks writes when set, which is Master/Power On reset default]
5	-	First byte of data to send to flash
|	|	|
N	-	Last byte of data to send to flash

Figure 3 Write External Flash Message Format

Bytes 2 and 3 specify the number of bytes remaining in the message. The CTRL byte definition is shown below.

CTRL[7:2] Reserved
CTRL[1] Write Protect – if set asserts WR_PROTECT_N to the flash
CTRL[0] Flash Hold CS – if set CS is left active at the end of the command

Read External Flash

The Read External Flash message is used to read data from an external flash device. Reading data from the flash requires first sending the read command and starting address to the flash using the Write External Flash command. This command is valid only when the sensor is in idle mode and the USB interface is selected. The Read External Flash message is shown in Figure 4.

Byte	Value	Description
1	0x41	Read External Flash command
2	0x00	Upper byte of number of bytes to follow
3	0x03	Lower byte of number of bytes to follow
4	CTRL	Control for SF_WP and SF_CS_N
5	CNT_H	Upper byte of number of bytes to read from flash
6	CNT_L	Lower byte of number of bytes to read from flash

Figure 4 Read External Flash Message Format

Bytes 2 and 3 specify the number of bytes remaining in the message. For the Read External Flash message this is always 3. The CTRL byte definition is shown below. Bytes 5 and 6 specify *m*, the number of bytes to be read from the flash.

CTRL[7:2] Reserved
CTRL[1] Write Protect – if set asserts WR_PROTECT_N to the flash
CTRL[0] Flash Hold CS – if set CS is left active at the end of the command

Write RISC Program RAM

The Write RISC Program RAM message is used to load a patch into the RISC Program RAM. This command is valid only when the sensor is in idle mode. The Write RISC Program RAM message is shown in Figure 5.

Byte	Value	Description
1	0x42	Write RISC Program RAM command
2	LEN_H	Upper byte of number of bytes to follow
3	LEN_L	Lower byte of number of bytes to follow
4	ADDR_H	Upper byte of starting address
5	ADDR_L	Lower byte of starting address
6	DATA1	Upper nibble of first word to write to Program RAM
7	DATA2	Lower nibble of first word to write to Program RAM
N	DATAM	Lower nibble of last word to write to Program RAM

Figure 5 Write RISC Program RAM Message Format

Bytes 2 and 3 specify the number of bytes remaining in the message. The starting address to be written to is specified in bytes 4 and 5 (ADDR_H is the high byte). DATA1 is written is to the upper byte of the address specified in the Program RAM (mapped to

addresses beginning at 0x2000 in the RISC address space) and DATA2 is written to the lower byte. After writing RISC Program RAM, an Enable Patch message is required to specify the program address to be re-vectored and the destination address.

Read RISC Program RAM

The Read RISC Program RAM message is used to read data from the RISC Program RAM. This command is valid only when the sensor is in idle mode. The Read RISC Program RAM message is shown in Figure 6.

Byte	Value	Description
1	0x43	Read RISC Program RAM command
2	0x00	Upper byte of number of bytes to follow
3	0x04	Lower byte of number of bytes to follow
4	ADDR_H	Upper byte of starting address
5	ADDR L	Lower byte of starting address
6	CNT_H	Upper byte of number of words to read from RAM
7	CNT_L	Lower byte of number of words to read from RAM

Figure 6 Read RISC Program RAM Message Format

Bytes 2 and 3 specify the number of bytes remaining in the message. For the Read RISC Program RAM message this is always 4. The starting address to be read is specified in bytes 4 and 5 (ADDRh is the high byte). The number of words to be read is specified by *m*, the value contained in bytes 6 and 7. The sensor will respond to this message by sending a RISC Program RAM Message. The number of bytes returned will be twice the number of words read.

Enable Patch

The Enable Patch command enables instruction fetches from ROM to be replaced with a jump to routines downloaded to RAM. The patch must be downloaded to RAM before enabling the patch. The hardware supports re-vectoring of up to 8 addresses.

Byte	Value	Description
1	0x5A	Enable Patch Command
2	0x00	Upper byte of number of bytes to follow
3	0x05	Lower byte of number of bytes to follow
4	PATCHID	Specifies patch vector to select (0-7)
4	ADDR_H	Upper byte of address to be patched
5	ADDR L	Lower byte of address to be patched
6	DEST_H	Upper byte of destination address
7	DEST_L	Lower byte of destination address

Table 6 Enable Patch Command Message Format

Disable Patch
The Disable Patch command disables re-vectoring.

Byte	Value	Description
1	0x5B	Disable Patch Command
2	0x00	Upper byte of number of bytes to follow
3	0x01	Lower byte of number of bytes to follow
4	PATCHID	Specifies patch vector to disable (0-7)

Table 7 Disable Patch Command Message Format

Load Offset Cal Table
The Load Offset Cal Table command can be used to update the sensors Offset Cal Table. The Offset Cal table specifies the OFFDAC BASE (REGAE) setting to be used for each gain setting. The sensor will automatically set the OFFDAC BASE register to the table value after gain is programmed unless DISABLE AUTO OFFDAC (REG8A[6]) is set or the sensor has been placed in Skip Offset Cal Test Mode.

Byte	Value	Description
1	0x5C	Load Offset Cal Table Command
2	0x00	Upper byte of number of bytes to follow
3	0x10	Lower byte of number of bytes to follow
4	OFFSET_0	OFFDAC BASE setting to use for Gain 0
5	OFFSET_1	OFFDAC BASE setting to use for Gain 1
19	OFFSET_F	OFFDAC BASE setting to use for Gain F

Table 8 Load Offset Cal Table Command Message Format

Register Write Message
Writing to a sensor register requires first sending a byte that selects the register followed by the value to write to the register. The Register Write Message is shown below.

Byte	Value	Description
1	REG ID	Sensor register address to write (0x80 to 0xDF)
2	DATA	Byte to write to sensor register

Figure 7 Register Write Message Format

If the first byte written is a 0xFF the sensor ignores it and waits for a valid register address. This provides a mechanism to recover if the software does not know whether the sensor is waiting for a header or data. Writing the sequence 0xFF, 0x80, 0x01 will always perform a master reset.

Data From Sensor

Each message from the sensor is preceded by a one-byte header that identifies the message type and allows the message length to be determined. Table 8 shows valid sensor data messages. In Imaging or Navigation modes, each image data frame can produce an E-field Data Message, a Histogram Message, and an Authentication Message in that order. Messages are sent when enabled (REG8F). For Impedance data see the Bussed Pixel Table Message description. A debug mode for Impedance is provided that returns measured data every frame. If Impedance debug Mode is enabled, Impedance Debug messages are sent as the last message of the frame.

Message ID	Message Contents
0x04	BIST Results Message
0x80-0xBF	Register Data
0xD0	External Flash Data
0xD1	RISC Program RAM Data
0xD2	Bussed Pixel Reference Table
0xD3	Bussed Pixel Measured Table
0xD8	Cal Data Message
0xD9	Debug Message
0xDE	Histogram
0xDF	Authentication
0xE0	4-bit E-field Data
0xE4	1-bit E-field Data
0xE8	2-bit E-field Data
0xEC	8-bit E-field Data

Table 9 Sensor Output Header Byte Definition

Register Data Message

Register data is sent in response to a read registers request (initiated by writing 0x81, 0x02 to the sensor) or at the end of an image slice. The Register Data Message is shown in Figure 9.

Byte	Value	Description
1	0x80	Load Offset Cal Table Command
2,3	0x003F or 0x0060	Bytes remaining in message
3	REG80	Contents of REG80
4	REG81	Contents of REG81
	|	|
65	REGBE	Contents of REGBE

Figure 8 Register Data Message Format

Bytes 2 and 3 specify *n*, the number of bytes remaining in the message. For the Register Data message this is either 63 or 96 depending on whether the Ext Reg Enable bit in REG80 is low or high.

Some of the commands initiated by writing to REG81 return a 2 byte register message consisting of a single register header followed by the register contents. In addition a single register can be read be writing the controls in REG8D and REG8F. If the single register is 0x80, the read will include a length field in addition to the data value. If the single register is any other register the sensor will send two bytes with the first byte being the register address (in the range 0x81 to 0xCF) and the second byte being the register contents. Single register reads for registers in the range 0xD0-0xDF is not supported since those register headers are the same as headers for other messages.

E-field Data Message

The E-field Data Message is sent when imaging. Definitions for the header bytes are shown in Table 9. The byte count *n* specified in bytes 2 and 3 is the number of bytes remaining (beginning with byte 4 of the message).

Byte	Definition
1	Message Type 0xE0 = 4-bit E-field data 0xE4 = 1-bit E-field data 0xE8 = 2-bit E-field data 0xEC = 8-bit E-field data
2	Number of bytes to follow MSB
3	Number of bytes to follow LSB
4	Header Version (definition below is version 0)
5	Frame Number MSB
6	Frame Number LSB
7	X-movement since last E-field slice (signed 8-bit value)
8	Y-movement since last E-field slice (signed 8-bit value)
9	Upper byte of Start Of Frame timestamp (1 us resolution)
10	Lower byte of Start Of Frame timestamp (1 us resolution)
11	Upper byte of End Of Frame timestamp (1 us resolution)
12	Lower byte of End Of Frame timestamp (1 us resolution)
13	E-field Settings 1 (REG83)
14	E-field Settings 2 (REG8A)
15	E-field Settings 3 (REG8B)
16	E-field Settings 4 (REG8C)
17	E-field Settings 5 (REG8E)
18	E-field Settings 6 (REG90)
19	E-field Settings 7 (REG91)
20	E-field Settings 8 (REG92)
21	E-field Settings 9 (REGA6)
22	E-field Settings 10 (REGAE)
23	E-field Settings 11 (REGBF)
24	E-field Settings 12 (REG95)
25	E-field Settings 13 (REG96)
26	E-field Settings 14 (IMAGE_PWR_H)
27	E-field Settings 15 (IMAGE_PWR_L)
28	Reference X
29	Reference Y
30	Skew
31	RSR Status Bit 0 – High indicates break.
32	Reserved (WHT_VALUE for HGC, AVGPIX for NGC)
33	Reserved (BLK_VALUE for HGC, MEDIX for NGC)
34-N	Sensor Data

Table 10 E-field Header Version 0 Definition

E-field Pixel data is sent in column order so that the first data is for the pixel at (x,y) location (0,0), the second is for location (0,1), and so on.

Table 10 shows how E-field pixel data is packed into bytes for various data formats and the length of E-field Sensor Data messages when the full array (1536 pixels) is scanned.

Format	First Byte	Length (bytes)
8-bit	[7:0] = pixel(0,0)	1569
4-bit	[7:4] = pixel(0,1) [3:0] = pixel(0,0)	801
2-bit	[7:6] = pixel(0,3) [5:4] = pixel(0,2) [3:2] = pixel(0,1) [1:0] = pixel(0,0)	417
1-bit	[7] = pixel(0,7) [6] = pixel(0,6) [5] = pixel(0,5) [4] = pixel(0,4) [3] = pixel(0,3) [2] = pixel(0,2) [1] = pixel(0,1) [0] = pixel(0,0)	225

Table 11 E-field Sensor Data Packing

Histogram Message

Histogram data is sent after image data (E-field) when histograms are enabled. The Histogram Message is shown in Figure 11.

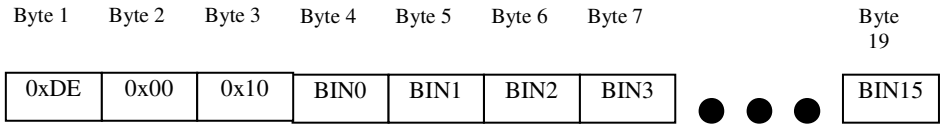


Figure 9 Histogram Message Format

The first byte sent from the sensor is the header (0xDE). The number of bytes to follow is specified by the value contained in bytes 2 and 3. For the Histogram message this is always 16. The next 16 bytes contain the values of each histogram BIN beginning with BIN0. The histograms are expressed in 128ths.

Authentication Message

Authentication data is sent after image data (E-field) when enabled. The Authentication Message is shown in Figure 12.

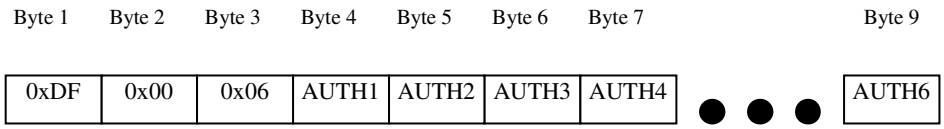


Figure 10 Authentication Message Format

The first byte sent from the sensor is the header (0xDF). The number of bytes to follow is specified by the value contained in bytes 2 and 3. For the Authentication message this is always 6. The next 6 bytes contain the authentication value calculated for the image. The authentication value returned is the actual 48-bit value. It is not padded with zeros to reach 64-bits as in earlier sensors.

External Flash Data Message

External Flash data is sent in response to the sensor being configured to read data from the external flash. The External Flash Data Message is shown in Figure 13.

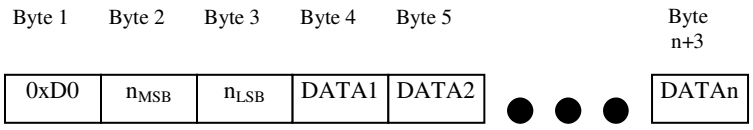


Figure 11 External Flash Data Message Format

The first byte sent from the sensor is the header (0xD0). The number of bytes to follow is specified by *n* (the value contained in bytes 2 and 3). The External Flash Data message is *n*+3 bytes in length.

RISC Program RAM Data Message

RISC Program RAM data is sent in response to the sensor being configured to read data from Program RAM. The RISC Program RAM Data Message is shown in Figure 14.

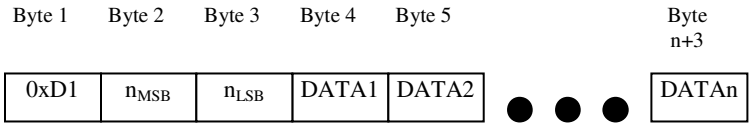


Figure 12 RISC Program RAM Message Format

The first byte sent from the sensor is the header (0xD1). The number of bytes to follow is specified by *n* (the value contained in bytes 2 and 3). The RISC Program RAM Data message is *n*+3 bytes in length.

Bussed Pixel Table Message

NOTE: The proposed message format is described below and is not part of the A0 ROM code. It should be considered subject to change until the implementation is complete. Bussed Pixel Table messages are sent when Bussed Pixel Data is enabled and a valid table has been completed. The Bussed Pixel Table Message is shown in Figure 15. When Impedence Mode is enabled (REGA2), bussed pixel data is measured every frame and returned to the host only when a table (consisting of measured data for all programmed frequencies and phases) is complete. The number of frames needed to complete the table is not deterministic due to potential gain adjustments that cause the data collection to restart.

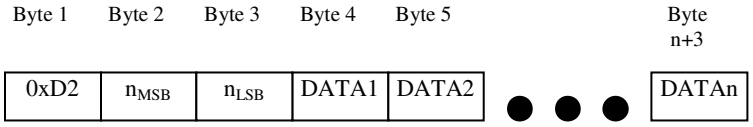


Figure 13 Bussed Pixel Table Message Format

The first byte sent from the sensor is the header (0xD2 or 0xD3). The number of bytes to follow is specified by *n* (the value contained in bytes 2 and 3). Table 11 shows byte definitions for the bussed pixel table.

Byte	Definition
1	Message Type 0xD2 = Bussed Pixel Reference Table 0xD3 = Bussed Pixel Measured Table
2	Number of bytes to follow MSB
3	Number of bytes to follow LSB
4	Bussed Pixel Settings 1 REGC1
5	Bussed Pixel Settings 2 REGC3
6	Bussed Pixel Settings 3 REGC4
7	Bussed Pixel Settings 4 REGC5
8	Bussed Pixel Settings 5 Samples Per Sweep
9	Bussed Pixel Settings 4 REGCB
10	Bussed Pixel Settings 4 REGCD
11	Value for Freq 1, Phase 1
|	|
18	Value for Freq 1, Phase 8
19	Value for Freq 2, Phase 1
|	|
26	Value for Freq 2, Phase 8
27	Value for Freq 3, Phase 1
|	|
34	Value for Freq 3, Phase 8
35	Value for Freq 4, Phase 1
|	|
42	Value for Freq 4, Phase 8
43	Value for Freq 5, Phase 1
|	|
50	Value for Freq 5, Phase 8

Table 12 Bussed Pixel Message Byte Definition

BIST Results Message

A BIST Results message is sent in response to the Run BIST command. The BIST Results Message is shown in Figure 16.

Byte	Value	Description
1	0x04	BIST Results message ID
2	0x00	Upper byte of number of bytes to follow
3	0x03	Lower byte of number of bytes to follow
4	STATUS	BIST Results 0x00 = Passed 0x01 = ROM Test Failed 0x02 = INBUF Test Failed 0x03 = BUF Test Failed
5	DATA_H	Upper byte of returned data
6	DATA L	Lower byte of returned data

Figure 14 BIST Results Message Format

The first byte sent from the sensor is the header (0x04). The number of bytes to follow is specified by the value contained in bytes 2 and 3. For the BIST Results message this is always 3. The BIST status is in Byte 4. A non-zero status indicates that a BIST test failed. When BIST passes, bytes 5 and 6 are not used and will return zeros. If the ROM test fails, bytes 5 and 6 indicate the calculated checksum. If a RAM test fails, bytes 5 and 6 indicate the failing address. INBUF is in the address range 0x1000-0x1FFF and BUF is in the address range 0x2000-0x3FFF.

Some failure modes (e.g. an unreadable ROM) will result in the Run BIST command not completing. The Run BIST test should be considered failing if the command does not return results within 50 ms.

Cal Data Message

A Cal Data message is sent in response to the Read Offset Cal Table command. This allows the host to read the calibration data that the sensor is currently using. The sensor performs Calibration in response to a Run Cal command. The Cal Data Message is shown in Figure 17. Note that the Cal Data Message format is changed in A1 silicon or A0 silicon when using a0a1_patch.c version 3 or higher. The A0 ROM version does not return the REGD0 or REGAF settings.

Byte	Value	Description
1	0xD8	Offset Cal Table message ID
2	0x00	Upper byte of number of bytes to follow
3	0x12	Lower byte of number of bytes to follow
4	OFFSET_0	OFFDAC BASE setting used for Gain 0
5	OFFSET_1	OFFDAC BASE setting used for Gain 1
	|	|
19	OFFSET_F	OFFDAC BASE setting used for Gain F
20	REGD0	LPO FREQ ADJUST setting (REGD0[4:0])
21	REGAF	FD THRESHOLD DAC setting

Figure 15 Cal Data Message Format

Sensor Register Map

The FPS19 Sensor Register Map is shown below. In the Reset column P indicates Power On Reset, M is Master Reset. Highlighted registers indicate differences from 1710.

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Reset	
0x80	Ext Reg Enable	Auto Restart FD	Sensor Mode [1:0]		HGC Enable	LPO Start	Force Finger On	Master Reset[1,4]	0x00	M
0x81	Run BIST[4]	Run Timer[4]	Run Cal[4]	Read ID[4]	Run FD[4]	N-shot[4]	Read Reg[1,4]	Cont Scan	0x00	M
0x82									0x02	P
0x83[2]	Finger Present[2]	Frame Rate Not Met[2]	Mult Updated[2]	Gain OK[2]	Cont Done[2]	Timer Idle[2]	Interference[2]	NVM TM5[2]	0xXX	-
0x84	N-Shot Count[7:0]								0x01	M
0x85	Flush Per Frame	-	-	-					0x00	P
0x86	-	-							0x00	P
0x87	Finger On Threshold[7:0]								0x32	M
0x88	Run On [7:0]								0xC8	M
0x89	FD Off Threshold[7:0]								0x64	M
0x8A	Update At Mult / Mult Updated[2]	Disable Auto Offdac	FD Sel[1:0]		-	Excite Mode [2:0]			0x07	M
0x8B	Excite Cycle[2:0]			Excite Freq[4:0]					0x0E	M
0x8C	Excite Phase [7:0]								0x60	M
0x8D	Single Reg ID [7:0]								0x00	M
0x8E	E-field Uber Gain Disable	Excite Drive [2:0]			E-field Uber Gain[3:0]				0x56	M
0x8F	-	Single Reg En	-	HISTO 64	EHISTO DIS	AUTH DIS	EDATA DIS		0x00	M
0x90	OFFSET [7:0]								0x00	M
0x91	MULT [7:0]								0x08	M
0x92	EGAIN3[1:0]		EGAIN2 [2:0]			EGAIN1 [2:0]			0x81	M
0x93[2]	Frame Number [7:0][2]								0x00	M
0x94[2]	Frame Number [15:8][2]								0x00	M
0x95	-	EPIX AVG [2:0]			Col Scanned [3:0]				0x08	M
0x96	-	COL OFFSET [6:0]							0x00	M
0x97	-	-	EPIX DEPTH [1:0]		EBIN THRESH [3:0]				0x08	M
0x98	Frame Rate[15:8][1] / Nav Time Base[7:0][1]/Frame Start[15:8][2]								0x00	M
0x99	Frame Rate[7:0][1] / Nav Repeat[7:0][1]/Frame Start[7:0][2]								0x00	M
0x9A	Nav Mult[7:0][1]/Frame End[15:8][2]								0x00	M
0x9B	Frame End[7:0][2]								0x00	M
0x9C	Ch Word[31:24][1], Foundry[3:0][2]								0x00	M
0x9D[2]	Ch Word[23:16][1]/ChipID [7:0][2]								0x19	M
0x9E[2]	Ch Word[15:8][1]/ IO_SEL[2]								0x00	M
0x9F[2]	Ch Word[7:0][1]/Mask Rev [7:0][2]								0x00	M

Table 13 Standard Registers Summary

[1]Write Only
[2]Read Only
[3]Power On Reset
[4]Self Resetting

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Reset	
0xA0	Read Buffered Egain	FSHR Spare[6:0]							0x00	M
0xA1	Sel NCO Clk		Excite Test En	Excite Test Data[4:0]					0x00	M
0xA2	VTERM On During Xmit	BIT Clk On	BIT DCRSTR	ROW DCRSTR	ATE Skip Analog Reset	Limit Drive	Imp Mode	BIT Analog On	0x00	M
0xA3	A2DDc_Test[3:0]				Arydc Test[3:0]				0x00	M
0xA4	Excite pd	Ary pd	A2d pd	A2Ddig1_en	A2Ddig1_test [3:0]				0x00	M
0xA5	A2DAc_Test[3:0]				A2DAc_En	A2Ddig2_en	A2Ddig2_test [1:0]		0x00	M
0xA6	FloatN	HiGv[1:0]		FRSR[63:62]		Nvm_test_n	FD LPNAV pd	SWSHR[16]	0xA6	M
0xA7	Lvshift	Sense Amp pd	SE Mode	Arydig_en	Arydig_test [3:0]				0x80	M
0xA8		Invert BIT Data	Fixed BIT Data	Dig BIT En	Dig Bit Data [4:0]				0x00	M
0xA9	Dig Mux 0 En	Dig Mux 0 Sel [6:0]							0x00	P
0xAA	Dig Mux 1 En	Dig Mux 1 Sel [6:0]							0x00	P
0xAB	Dig Mux 2 En	Dig Mux 2 Sel [6:0]							0x00	P
0xAC	Clk Keep On [7:0]								0x00	P
0xAD	-	ADVrange 2V	-	-	LPFD Sample Early	LPFD avg[2:0]			0x00	M
0xAE	OFFDAC Base[7:0]								0x80	M
0xAF	FD THRESH DAC [7:0]								0x80	P
0xB0	-	GPO Disable [2:0]			-	GPO[2:0][1]/GPI[2:0][2]			0xFX	P
0xB1	SENSOR RESET	-	Orig Embd Word	Test Embd Word	Analog pd	Analog Reset	ATE Cont. Image	-	0x00	M
0xB2	LPO Coarse[1:0]		-	A2D Spare[4:2]			FD OFF D2A SEL	FD HYS EN	0x40	M
0xB3	Startup Dly [7:0]								0x32	P
0xB4	-	-	-	Single CDS En	CDS[3:0]				0x00	M
0xB5	Idac[1:0]		Ivrpix [1:0]		Ivrcm[1:0]		Isense amp [1:0]		0xAB	M
0xB6	SHIFT CDS	ALT MULT UPDATED			Ianch [1:0]		Icdsamp [1:0]		0x0A	M
0xB7	SA8_TMB	V2X_SPARE2						LOAD SR[4]	0x80	M
0xB8	-	FNGRDrvBias[2:0]			MTC SEL[1:0]		FRSR[32:31]		0x40	M
0xB9	PLL On Delay[3:0]				Osc On Delay [3:0] [2,3]				0x24	P
0xBA	SWSHR[14]	-	BPR HIGV[1:0]		Buffer Flush[4]		SEND FRSR[4]	SEND SWSHR[4]	0x00	M
0xBB	-	Analog Test Mode	Analog TM[5:0]						0x04	M
0xBC	A2D Clk Sel[1:0]		Excite Spare[2]	**COPY HIGV[1:0]**	A2D BGtrim [2:0]				0x04	M
0xBD	LPO In [15:8]								0x13	M
0xBE	LPO In [7:0]								0x88	M
0xBF			Quadrature Mode	Noise Floor Mode	RSR DIR[1:0]		RSR LEVEL[1:0]		0x10	M

Table 14 Test Registers Summary

[1]Write Only
[2]Read Only
[3]Power On Reset
[4]Self Resetting

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Reset	
0xC0	BP Excite Cycle[2:0]			BP Init Freq[4:0]					0x0D	M
0xC1	BP Phase Step[7:0]								0x08	M
0xC2	BP Pixel Avg[2:0]			BP Gain Inc[1:0]		VCM DCRSTR	VCM State	Bussed Pixel Enable	0x92	M
0xC3	BP Phase Init[7:0]								0x08	M
0xC4	BP Freq Start[3:0]				BP Freq Stop[3:0]				0xDF	M
0xC5	BP Gain[3:0]				Fixed BP Gain	BPR Excite Drive[2:0]			0xF2	M
0xC6	BP Phase Stop[7:0]								0xB0	M
0xC7	BP Phase Loop Pnt[7:0]								0xB8	M
0xC8	BP Phase Loop Val[7:0]								0x50	M
0xC9	BP Offdac[7:0]								0x80	M
0xCA	FRSR[57:56][20:15]								0x80	M
0xCB	BPRGAIN3 [1:0]		BPRGAIN2 [2:0]			BPRGAIN1 [2:0]			0x02	M
0xCC	FRSR[54][44:38]								0x00	M
0xCD	BPR Offdac[7:0]								0x80	M
0xCE			USE BPR REG	USE BP REG		BP FDRV BIAS[1:0]			0x03	M
0xCF	Frame Valid	Interference Avg[2]	Interference Avg.[1]	Interference Avg.[0]/ SEL 1P5 CYCLES	EXCITE DELAY [3]	EXCITE DELAY [2]	EXCITE DELAY [1]/Interference Average Enable	EXCITE DELAY [0]/Interference Check Enable	0x04	M
0xD0	CDS Test Mode			LPO Freq Adjust[4:0][3]					0x10	M
0xD1		BPR PD			Row Offset Disable	-	V2X Clk Sel[1:0]		0x00	M
0xD2	Row 0 Offset [3:0]				Row 1 Offset [3:0]				0x00	P
0xD3	Row 2 Offset [3:0]				Row 3 Offset [3:0]				0x00	P
0xD4	Row 4 Offset [3:0]				Row 5 Offset [3:0]				0x00	P
0xD5	Row 6 Offset [3:0]				Row 7 Offset [3:0]				0x00	P
0xD6	Row En[7:0]								0xFF	M
0xD7	MAX PD INT [7:0]								0x20	M
0xD8	MAX PD FRAC [15:8]								0x00	M
0xD9	MAX PD FRAC [7:0]								0x00	M
0xDA			BP HiGv[1:0]			BP Excite Drive[2:0]			0x00	M
0xDB	BPGAIN3[1:0]		BPGAIN2[2:0]			BPGAIN1[2:0]			0x00	M
0xDC	DEBUG CTRL2[4:0]					BP Num Ref Sweep[2:0]			0x07	M
0xDD	DEBUG CTRL1[7:0]								0x00	M
0xDE	Synth NCO TM[2:0]			NCO Clk Cnt[12:8] [3]					0x10	M
0xDF	NCO Clk Cnt[7:0] [3]								0x00	M

Table 15 Extended Registers Summary

[1]Write Only
[2]Read Only
[3]Power On Reset
[4]Self Resetting

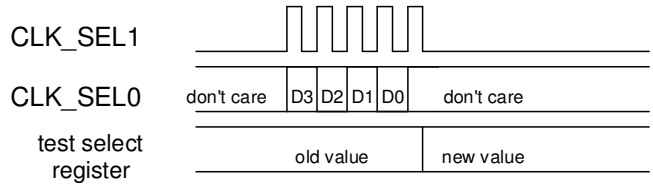
Detailed descriptions for the fields in each register are provided in Appendix A. During image data acquisition register writes are buffered. Sensor Registers are updated between image frames. E-Field Gain Registers are all updated at the same time if Update At Mult is set.

Digital Test Modes

The Idaho[AES2550] Digital Test Mode implementation requires a single dedicated pin: TEST_MODE.

When the TEST_MODE pin is low all test control signals are forced to their inactive state. The state mode used to acquire data is kept in the reset state.

When the TEST_MODE pin is high the CLK_SEL pins are used to update an internal register that is used to select between the various test modes. Five clocks are required to update the test select register as shown in the figure below. The first 4 clocks shift data in. The host shifts new data out coincident with the rising edge of the clock. The test controller logic samples the data using the falling edge of the clock.



Internally the CLK_SEL pin states present before the TEST_MODE pin was brought high are held so that the PLL is not affected by clocking data into the test select register.

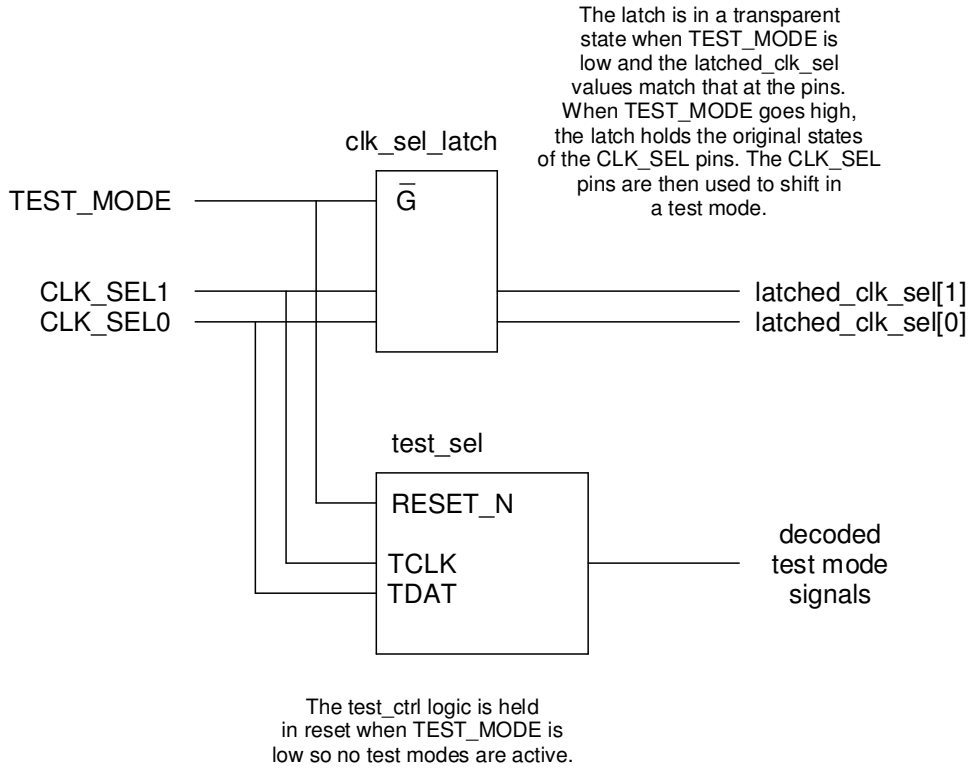


Table 12 shows how the test select values are decoded into the various test modes.

Test Select	SLEEP_N	Name	GPO_EN[2:0]	SCAN_MODE	SCAN_EN	CLK_DISABLE	OSC_DISABLE	PLL_DISABLE	LPO_CLK_EN	LPO_DISABLE	FORCE_FP	SENSOR_MODE[1:0]	SO_OE_N[10:0]	ANALOG_PD	USB_SUSPEND	USB_OE_N
0000b	1	Clock View	111b	0	0	0	0	0	1	0	-	-	-	-	-	-
0000b	0	Dynamic Burn In	-	0	0	-	-	-	1	0	1	01b	-	-	-	-
0001b	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-
0010b	-	Nandtree	-	0	0	1	0	-	1	0	-	-	0x3FF	1	-	-
0011b	-	Scan	-	1	0	0	0	0	1	0	-	-	-	1	-	-
0100b	-	Reserved	-	-	-	-	-	-	-	-	-	-	-	1	-	-
0101b	-	USB Xcvr	000b	0	0	0	0	0	1	0	-	-	-	1	0	0
0110b	-	USB Suspend	111b	0	0	1	1	1	1	0	-	-	-	1	1	1
0111b	-	Leakage	111b	0	0	1	1	1	0	1	-	-	-	1	1	1
1000b	-	LPO Current	111b	0	0	1	1	1	0	0	-	-	-	1	1	1
1001b	-	LPO and Clock Load	111b	0	0	1	1	1	1	0	-	-	-	1	1	1
1010b	-	Oscillator Current	111b	0	0	1	0	1	0	1	-	-	-	1	1	1
1011b	-	Oscillator and PLL Current	111b	0	0	1	0	0	0	1	-	-	-	-	1	1
1100b	-	Skip Offset Cal	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1101b	-	Reserved	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1110b	-	Reserved	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1111b	-	Reserved	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 16 Digital Test Mode Controls

Functional descriptions for each of the decoded test modes is shown below. Many of the test modes utilized on the ATE will also require that the sensor be in PLL Bypass mode so that the sensor outputs are synchronized to the tester. PLL Bypass will be enabled separately by appropriate setting of the CLK_SEL pins.

Clock View

This mode configures the test mux and enables GPO pins to allow viewing the oscillator, PLL, and LPO signals. Pin definitions are as shown in the table below.

Signal	Pad	Pin
XTAL Oscillator	SIO[8]	GPIO[0]
PLL	SIO[9]	GPIO[1]
Low Power Oscillator	SIO[10]	GPIO[2]

Since the test select logic is kept in the reset state when the TEST_MODE pin is low, this mode is enabled solely by setting the TEST_MODE pin high. If the interface selected has

a SLEEP_N pin it must be in the high state. This mode cannot be used to view the power up response of the clocks since TEST_MODE must be low after power up to get the test select registers in the correct state. TEST_MODE can go high before or after RESET_N since the test mode logic is not affected by RESET_N.

Dynamic Burn-In
This mode configures the sensor into imaging mode at the fastest rate possible. It is intended to be used during Dynamic Burn-In to allow the part to be configured without sending any commands.

Since the test select logic is kept in the reset state when the TEST_MODE pin is low, this mode is enabled by setting the TEST_MODE pin high. The interface selected must have a SLEEP_N pin and it must be set to the low state. In this mode it does not shut off the xtal oscillator or PLL. Since there is no need to shift in data the mode is easily enabled on a burn in board. TEST_MODE must be set high after RESET_N is high.

Nandtree
This allows easy characterization of input switching thresholds. The sensor is placed into the suspend state to allow quick ATE measurement of suspend current. TEST_MODE and CLK_SEL pins are not included in the nandtree. RESET_N, IO_SEL, SIO_0, SIO_1, …, SIO_9 pins are the inputs (in that order) and SIO_10 is the output.

Scan
When Scan is selected CLK_SEL0 is used as SCAN_EN.

When SCAN_EN is high the registers in each scan chain are placed into shift mode. This is used to shift in new states and shift out existing states. The table below shows how pins are re-defined when SCAN_EN is high.

Scan In	Length	Scan Out
IO_SEL	TBD	SIO[5]
SIO[0]	TBD	SIO[6]
SIO[1]	TBD	SIO[7]
SIO[2]	TBD	SIO[8]
SIO[3]	TBD	SIO[9]
SIO[4]	TBD	SIO[10]

When SCAN_EN is low all logic and I/O are in functional states except bypass logic on RAM/ROM, test stimulus registers, and asynchronous path blocking. SCAN_MODE is asserted. This is used to capture logic responses from shifted in states.

Detailed requirements for the SCAN_MODE and SCAN_EN signals are listed below.

- SCAN_MODE. When active it should
    - Substitute CLK48MHZ for LPO_CLK. The mux that does this should be such that when the CLK48MHZ path is selected the insertion delay is the same as for the other clock paths.

- Enable all clocks all the time. With the exception of LPO_CLK, all clocks are gated versions of CLK48MHZ. When SCAN_MODE is active all clocks are CLK48MHZ.
- Disable any oscillator, pll, or clock controls so that the clock path from XTALIN remains inactive regardless of any register states. This includes at least CLK_STANDBY and OSC_DISABLE.
- Keep the PLL in bypass mode. This can also be accommodated by requiring the CLK_SEL pins be set appropriately.
- Keep power down signals to the analog circuits active so that the analog circuits remain in their low power states. This prevents large current spikes (and the associated noise) from occurring during digital testing.
- Enable "shadow registers" that will substitute signals from registers (that are part of the scan chain) in place of signals that normally come from analog circuits. Shadow registers will also be used to capture the states of control signals to the analog circuits.
- Enable pass-thru modes for modules that will be treated as "black boxes" during ATPG. This would typically include and ROM and RAM modules.
- IO pins should maintain the same functionality as for normal operation to allow for maximum fault coverage from the automatically generated scan patterns.

- SCAN_EN. When active it should
  - Reconfigure digital logic into shift registers to allow shifting in new states while testing current states.
  - Force any bi-directional pins to be outputs. **Note: Need to make sure that FastScan can handle bi-directional SCAN_IN or SCAN_OUT pins. It may be necessary to move this requirement to the SCAN_MODE signal so that pin directions are fixed for ATPG.**

USB Xcvr

Used for ATE testing of the USB Transceiver. The table below shows how transceiver pins are mapped.

Signal	Dir	Pin
DPLUS	I/O	SIO[0]
DMINUS	I/O	SIO[1]
USB_OEN	I	SIO[2]
USB_SUSPEND	I	SIO[3]
USB_VPO	I	SIO[4]
USB_VMO	I	SIO[5]
USB_RCV	O	SIO[6]
USB_VP	O	SIO[7]
USB_VM	O	SIO[8]

A clock is required since the transceiver re-clocks USB_VPO, USB_VMO, and USB_OE_N to minimize skew.

Module Requirements

Low Power Oscillator

The Low power oscillator will have an 5-bit control that allows it to be adjusted to 20 KHZ with an accuracy of no greater than +/- 10 %.

Reset

Power On Reset goes active asynchronously when the RESET_N pin is low. It goes inactive synchronously two clocks after reset is released.

Master Reset goes active when Power On Reset is active or when the Master Reset bit in REG80 is written with the D0 bit set and SCAN_MODE is not active.

Oscillator/PLL Startup and controls

The oscillator is required to startup in less than 3 ms. This startup time must be met over expected sensor variations over process, voltage, and temperature. The oscillator must work properly with a wide range of board capacitances (1-20 pf), a wide range of crystal Q values (xx-xxx) and capacitances. It must also work with ceramic resonators.

The PLL is required to startup and lock in less than 100 us. This specification must be met over all process, voltage, and temperature conditions.

When the RESET_N pin is low the oscillator and PLL are enabled and in an active state. RESET_N must be held active for 3ms minimum to allow the oscillator to start (3 ms max). The oscillator must function normally when RESET_N is active. The PLL is affected by RESET_N and does not start to lock until RESET_N goes high. Internal sensor clocks are kept disabled for 200 us nominally to allow the PLL to lock.

When the oscillator is turned on under sensor control the PLL is kept off for 3 ms and clocks to digital logic are disabled at the clk_ctrl module using CLK_STANDBY. After 3 ms the PLL is enabled and clocks remain gated off for an additional 200 us.

The PLL is required to support 4x multiplication and a bypass mode.

Oscillator and PLL controls are synchronized to provide synchronous turn off/asynchronous turn on.

Macro Test Chain

A macro test chain (mtc) is included to allow ATE measurements to be made characterizing gate delays. The mtc includes chains of 20 ND2 gates, 20 NR2 gates, and 10 FA1 gates along with a bypass path. Chain selection uses MTC SEL (REGB8[3:2]). The input to the mtc is from SIO_7 and the output is available via the digital test mux.

The MTC chain uses cells from the DIGALOG library.

Appendix A – Register Details

Detailed descriptions for Sensor Register bit fields are shown below.

REG80

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Ext Reg Enable	Auto Restart FD	Sensor Mode [1:0]		HGC Enable	LPO Start	Force Finger Present	Master Reset

Ext Reg Enable

Controls which registers are returned in response to a register read when Single Reg En (REG8F) is low.

0 Register reads include REG80-REGBE.
1 Register reads include REG80-REGDF.

Auto Restart FD

Controls what happens in Imaging or Nav using Cont Scan after Finger Off is detected.

0 Sensor clears Cont Scan, stops imaging, and waits for next command.
1 Sensor reloads REG81 with value at start of imaging. Run FD is always set on restart.

Sensor Mode [1:0]

00 Idle
01 Imaging. Can include interleaved bussed pixel.
10 Navigation
11 Reserved

HGC Enable

High enables RISC gain control.

LPO Start

When set this starts the sensor Low Power Oscillator (LPO) Timer. The timer delays the number of microseconds specified by the Frame Rate register (REG98 and REG99). When the timer is done the sensor will return the status register as a 2 byte message (0x83 followed by the contents of REG83). This bit is self-clearing.

Force Finger Present

High allows sensor to act as if finger was detected.

Master Reset

High initiates a master reset of the sensor. This bit is self-clearing and will always read back 0.

REG81

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Run BIST	Run Timer	Run Cal	Read ID	Run FD	N-shot	Read Reg	Cont Scan

This register functions as a command register with each bit initiating a sensor action. To ensure correct operation writes to this register should initiate a single action. If multiple command bits are set they are prioritized with Run BIST (initiated by D7) being the highest priority and Read Reg (initiated by D2) being the lowest.

Run BIST

When set this initiates a test of RISC ROM, RISC and buffer RAM, and other TDB items. When the test is complete the sensor will return the status register as a 2 byte message (0x83 followed by the contents of REG83). This bit is self-clearing upon completion of the command. This command is only processed when the Sensor Mode (REG80) is set to Idle.

Run Timer

When set this starts the sensor Timer. The timer delays the number of microseconds specified by the Frame Rate register (REG98 and REG99). When the timer is done the sensor will return the status register as a 2 byte message (0x83 followed by the contents of REG83). This bit is self-clearing upon completion of the command. This command is only processed when the Sensor Mode (REG80) is set to Idle.

Run Cal

When set this initiates built in calibration. Exact details of calibrations performed are TBD but are expected to include the Low Power Oscillator (LPO), Offset DAC's (E-field, Bussed Pixel), and Low Power Finger Detect (LPFD) Threshold DAC. This bit is self-clearing upon completion of the command. This command is only processed when the Sensor Mode (REG80) is set to Idle.

Read ID

When set this initiates a read of the Sensor ID Register (REG9D). The sensor will return the Sensor ID Register as a 2 byte message (0x9D followed by the contents of REG9D). This bit is self-clearing upon completion of the command.

N-Shot

When set enables the sensor to send N images after a finger is detected. N is specified in REG84.

Read Reg

When set the sensor will return registers. The number of bytes returned for a read operation depends on the Single Reg En bit in REG8F and the Ext Reg Enable bit in REG80. upon completion of the command

Cont Scan

When high the sensor continuously send image slices when a finger is detected on the sensor. It will continue to send slices after finger detect is inactive for the number of slices specified by Run On Count in REG88. The total number of slices sent will be a modulo of the N-Shot Count setting (REG84).

REG82

This register is reset by Power On Reset. The reset value for this register is 0x02.

D7	D6	D5	D4	D3	D2	D1	D0

REG83

This register is a read-only status register. After a Master Reset the status should be 0x04.

D7	D6	D5	D4	D3	D2	D1	D0
Finger Present	Frame Rate Not Met	Mult Updated	Gain OK	Cont Done	Timer Idle	Interference	

Finger Present
When high a finger has been detected on the sensor.

Frame Rate Not Met
When high the sensor was not able to acquire image slices at the rate programmed in REG98 and REG99.

Mult Updated
When high the sensor was configured for Update At Mult, the mult register was written, and all the e-field gain registers have been updated on this image.

Gain OK
When high the sensor HGC algorithm has completed the initial gain adjustment.

Cont Done
When high this is the last image of an image obtained with Continuous. For continuous scan mode this indicates that a finger has been off the sensor for the number of frames set by RUN ON COUNT in REG88 and the number of frames delivered is a multiple of N-Shot Count.

Timer Idle
When high the timer is idle.

Interference
This bit is set when FD SEL (REG8A) is set to use Low Power Finger Detect with interference checks and interference is detected. The interference check looks for a received signal when no driving signal is supplied.

REG84

This register is reset by Master Reset. The reset value for this register is 0x01.

D7	D6	D5	D4	D3	D2	D1	D0
N-Shot Count[7:0]							

N-Shot Count[7:0]
Sets the number of frames that will be returned after the N-shot bit (REG81) is asserted and a finger is present. A zero value will result in 256 frames. In continuous can mode this register is used as a modulo counter and the number of image frames delivered will be an integral multiple of this value.

REG85

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Flush Per Frame	-	-					

Flush Per Frame

When this bit is set the USB interface will send a short packet at the end of each image frame. When cleared the USB interface will send a short packet at the end of a finger swipe..

REG86

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-				

REG87

This register is reset by Master Reset. The reset value for this register is 0x32.

D7	D6	D5	D4	D3	D2	D1	D0
Finger On Threshold[7:0]							

Finger On Threshold [7:0]

This controls the Finger On Threshold used when detecting a finger using image based finger detect.

REG88

This register is reset by Master Reset. The reset value for this register is 0xC8.

D7	D6	D5	D4	D3	D2	D1	D0
Run On [7:0]							

Run On [7:0]

This specifies the number of slices that should be taken after the frame where a finger is no longer detected on the sensor when operating in continuous scan mode.

REG89

This register is reset by Master Reset. The reset value for this register is 0x64.

D7	D6	D5	D4	D3	D2	D1	D0
FD Off Threshold[7:0]							

FD Off Threshold [7:0]

This allows adjusting the Finger Off Threshold used when detecting a finger using image based finger detect.

REG8A

This register is reset by Master Reset. The reset value for this register is 0x07.

D7	D6	D5	D4	D3	D2	D1	D0
Update At Mult / Mult Updated	Disable Auto Offdac	FD Sel[1:0]		-	Excite Mode [2:0]		

Update At Mult / Mult Updated

Used with Software Gain Control to force registers affecting E-Field Imaging to be updated at the same time (after the MULT register (REG91)) has been written. This bit is cleared when the gain registers are updated When read this bit returns Mult Updated. Mult Updated is high for one frame when Update At Mult is enabled, Mult has been written, and the gain registers are updated.

The registers that are buffered when this bit is set are REG8E, REG90, REG91, REG92, REGA6[6:5], REGAE, and REGB8[6:4].

0 Registers are updated between image frames.
1 Registers are updated after REG91 is written.

Disable Auto Offdac

Stops the sensor from automatically setting the OFFDAC BASE register (REGAE) after the gain register is set.

0 Sensor automatically sets OFFDAC BASE to table value after gain is programmed.
1 Sensor does not automatically set OFFDAC BASE.

FD Sel [1:0]

Selects the method used to detect a finger.

00 Edge Based (compare current image power to last image power)
01 Low Power Finger Detect (can be performed with clock off)
10 Reserved
11 Low Power Finger Detect with Interference Check

Excite Mode [2:0]

Specifies the signal used for to drive the FDRV pin

000 Sine
001 Pulse 1 48MHz clock wide
010 Pulse 2 48MHz clocks wide
011 Pulse 3 48MHz clocks wide
100 Pulse 4 48MHz clocks wide
101 Pulse 5 48MHz clocks wide
110 Pulse 6 48MHz clocks wide
111 Square

REG8B

This register is reset by Master Reset. The reset value for this register is 0x0E.

D7	D6	D5	D4	D3	D2	D1	D0
Excite Cycle[2:0]			Excite Freq[4:0]				

Excite Cycle [2:0]

Specifies the number of cycles in the interval when excitation is driven while imaging. The waveform driven by the excitation module is active for ½ cycle less. The CDS sample pulses occur during the last cycle.

000 2 excitation cycles
001 3 excitation cycles
010 4 excitation cycles
011 5 excitation cycles
100 6 excitation cycles
101 7 excitation cycles
110 8 excitation cycles
111 9 excitation cycles

Excite Freq [4:0]

Specifies the frequency of the excitation signal. For frequencies below 375 KHz the values shown below are rounded. The actual frequency is shown in parenthesis. These frequencies are accurate only when SYNTH INT (REGD7) is set to 0x20 and SYNTH FRAC (REGD8-REGD9) is set to 0x0000.

00000	91.552734375 Hz	(6 MHz / 65536)
00001	183.10546875 Hz	(6 MHz / 32768)
00010	366.2109375 Hz	(6 MHz / 16384)
00011	732.421875 Hz	(6 MHz / 8192)
00100	1.46484375 KHz	(6 MHz / 4096)
00101	2.9296875 KHz	(6 MHz / 2048)
00110	5.859375 KHz	(6 MHz / 1024)
00111	11.71875 KHz	(6 MHz / 512)
01000	23.4375 KHz	(6 MHz / 256)
01001	46.875 KHz	(6 MHz / 128)
01010	93.75 KHz	(6 MHz / 64)
01011	187.5 KHz	(6 MHz / 32)
01100	375 KHz	(6 MHz / 16)
01101	750 KHz	(6 MHz / 8)
01110	1.5 MHz	(6 MHz / 4)
01111	3.0 MHz	(6 MHz / 2)
10000	6.0 MHz	

REG8C

This register is reset by Master Reset. The reset value for this register is 0x60.

D7	D6	D5	D4	D3	D2	D1	D0
Excite Phase [7:0]							

Excite Phase [7:0]

Specifies the phase delay between the positive zero crossing of sine data and the falling edge of the CDS_SIGP sample pulse. This relation exists at the output of the digital subsystem and does not account for any delays through the excitation module. The register resolution is (360/256) degrees. The falling edge of the CDS_SIGM sample pulse always occurs 180 degrees after the CDS_SIGP sample pulse.

REG8D

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Single Reg ID [7:0]							

Single Reg ID [7:0]

Specifies the single register that should be returned in response to a Reg Read request or imaging/navigation slices with registers enabled. Valid values are 0x80-0xCF. Invalid values will result in the Chip ID register being returned (REG9D).

REG8E

This register is reset by Master Reset. The reset value for this register is 0x56.

D7	D6	D5	D4	D3	D2	D1	D0
E-field Uber Gain Disable	Excite Drive [2:0]			E-field Uber Gain[3:0]			

E-field Uber Gain Disable

When high the registers for Excite Drive, HiGv, and E-field Gain1, Gain2, and Gain3 are used. When low the E-field Uber Gain register is used to decode values for those registers.

Excite Drive [2:0]

Specifies the peak drive level for the excitation signal in sine mode.

000 1/32 * V2XOUT * 0.9
001 1/16 * V2XOUT * 0.9
010 1/8 * V2XOUT * 0.9
011 ¼ * V2XOUT * 0.9
100 ½ * V2XOUT * 0.9
101 V2XOUT * 0.9
110 V2XOUT * 0.9
111 V2XOUT * 0.9

E-field Uber Gain [3:0]

Controls all gain registers.

Drive	HiGv	Gain1	Gain2	Gain3		Total
0000	1/4	1x	1x	1x	1x	1/4
0001	1/2	1x	1x	1x	1x	1/2
0010	1	1x	1x	1x	1x	1
0011	1	2x	1x	1x	1x	2
0100	1	2x	1x	1x	2x	4
0101	1	2x	1x	1x	4x	8
0110	1	2x	2x	1x	4x	16
0111	1	2x	4x	1x	4x	32
1000	1	2x	8x	1x	4x	64
1001	1	2x	16x	1x	4x	128
1010	1	2x	16x	2x	4x	256
1011	1	2x	16x	4x	4x	512
1100	1	2x	16x	8x	4x	1024
1101	1	2x	16x	16x	4x	2048
1110	1	2x	16x	16x	4x	2048
1111	1	2x	16x	16x	4x	2048

REG8F

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
-	Single Reg En	-	HISTO64	EHISTO DIS	AUTH DIS	EDATA DIS	-

Single Reg En

In conjunction with Single Reg ID (REG8D), this allows reading a single sensor register.

0 Register Reads return multiple registers (quantity depends on Ext Reg Enable in REG80).

1 Register Reads return two bytes (Register Header and Register Data).

HISTO64

Defines the region to be histogrammed. For the histogram to be accurate and scaled correctly, the columns scanned must either fill or fit within the selected histogram region.

0 Histogram are obtained from the center 128 columns.

1 Histograms are obtained from the center 64 columns.

EHISTO DIS

Controls whether a histogram is sent with E-Field image frames. The histogram is generated from raw pixel data (before OFFSET and MULT are applied).

0 Histogram Messages are sent with each E-field image frame.

1 No E-field Histogram Messages are sent.

AUTH DIS

Controls whether authentication messages are sent with image data (E-Field).

0 Authentication Messages are sent with each image frame.

1 No Authentication Messages are sent.

EDATA DIS

Controls whether data is sent for E-Field image frames.

0 Data is sent for E-field image frames.

1 No data is sent for E-field image frames.

REG90

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
OFFSET [7:0]							

OFFSET [7:0]

Used as part of Histogram Correction function of gain control. The specified value is subtracted from each 8-bit E-field pixel value and the result is presented to the digital multiplier. The result of the subtraction is clamped at 0.

REG91

This register is reset by Master Reset. The reset value for this register is 0x08.

D7	D6	D5	D4	D3	D2	D1	D0
MULT [7:0]							

MULT [7:0]

Used as part of Histogram Correction function of gain control. After a pixel has the Digital Offset value subtracted from it the result is multiplied by the Digital Multiplier value. This value is in 5.3 fixed point format so that the reset value of 0x08 represents a multiplier value of 1.0. The result of the multiplication is clamped at 0xFF.

REG92

This register is reset by Master Reset. The reset value for this register is 0x81.

D7	D6	D5	D4	D3	D2	D1	D0
EGAIN3 [1:0]		EGAIN2 [2:0]			EGAIN1 [2:0]		

EGAIN3 [1:0]

Specifies the gain setting for the Offset Adjust and Level Shift amplifiers.

00 1X
01 2X
10 4X
11 4X

EGAIN2 [2:0]

Specifies the gain setting for the Second PGA.

000 1X
001 2X
010 4X
011 8X
100 16X
101 16X
110 16X
111 16X

EGAIN1 [2:0]

Specifies the gain setting for the First PGA.

000 1X
001 2X
010 4X
011 8X
100 16X
101 16X
110 16X
111 16X

REG93

This read only register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Frame Number [7:0][2]							

Frame Number [7:0]

This is the lower byte of the current frame number. The frame number is reset to 0 when a finger is first detected.

REG94

This read only register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Frame Number [15:8][2]							

Frame Number [15:8]

This is the upper byte of the current frame number. The frame number is reset to 0 when a finger is first detected.

REG95

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
-	EPIX AVG[2:0]			Col Scanned [3:0]			

EPIX AVG [2:0]

Specifies the number of times data is acquired from each column. The pixel data returned is the average of the sampled values.

0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128

Col Scanned [3:0]

Specifies the number of columns that will be scanned when the array is imaged. The scanned region is centered in the array when COL OFFSET (REG96) is set to 0.

Setting	Num Columns	Default Starting Column
0000	1	95
0001	2	95
0010	4	94
0011	8	92
0100	16	88
0101	32	80
0110	64	64
0111	128	32
1000	192	0

REG96

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
COL OFFSET [7:0]							

COL OFFSET [7:0]

Specifies an offset to be added to the default starting column for E-field data acquisition. See COL SCANNED in REG95 to determine default starting column based on COL SCANNED. If the resulting starting column is greater than the array size then the array size (192) is subtracted. This allows COL OFFSET to move the starting column both left and right.

REG97

This register is reset by Master Reset. The reset value for this register is 00h.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	EPIX DEPTH [1:0]		EBIN THRESH [3:0]			

EPIX DEPTH [1:0]

Specifies the number of bits that should be used to represent each pixel.

00 4-bit
01 1-bit
10 2-bit
11 8-bit

EBIN THRESH [3:0]

Specifies the threshold to be used when binarizing pixels. If the upper 4-bits of the 8-bit pixel value are greater than or equal to the value specified the binarized pixel will be a 1; if less than the value specified it will be 0.

REG98

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Frame Rate[15:8][1] / Nav Time Base[7:0][1]/Frame Start[15:8][2]							

Frame Rate [15:8]

When in imaging mode this register specifies the upper byte of the Frame Rate. The lower byte is specified in REG9A. This sets the time in microseconds from the start of one frame to the start of the next. If the programmed frame rate is not met the sensor will indicate that by setting the *Frame Rate Not Met* bit in REG83 and the image header.

Nav Time Base [7:0]

When in navigation mode this register specifies the time base in number of Low Power Oscillator (LPO) clocks. The LPO is calibrated to achieve a frequency of 20 KHz +/- 10%.

Frame Start [15:7]

When this register is read during imaging or navigation, it returns the upper byte of the Frame Start Time. The Frame Start Time is captured from a free-running timer with 1 us resolution.

REG99

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Frame Rate[7:0][1] / Nav Repeat[7:0][1]/Frame Start[7:0][2]							

Frame Rate [7:0]

When in imaging mode this register specifies the lower byte of the Frame Rate. The upper byte is specified in REG99. This sets the time in microseconds from the start of one frame to the start of the next. If the programmed frame rate is not met the sensor will indicate that by setting the *Frame Rate Not Met* bit in REG83 and the image header.

Nav Repeat [7:0]

When in navigation mode this register specifies the Nav Repeat value. The number of image frames acquired for a Nav Packet is this value plus one.

Frame Start [7:0]

When this register is read during imaging or navigation, it returns the lower byte of the Frame Start Time. The Frame Start Time is captured from a free-running timer with 1 us resolution.

REG9A

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Nav Mult[7:0] /Frame End[15:8][2]							

Nav Mult [7:0]

When in navigation mode this register specifies the multiplier that is applied to the Nav Time Base value to establish the time between the start of all image frames in the Nav Packet except the first. Nav Mult is specified in Fixed Point 7.1 format (7 integer bits, 1 fractional bit).

Frame End [15:8]

When this register is read during imaging or navigation, it returns the upper byte of the Frame End Time. The Frame End Time is captured from a free-running timer with 1 us resolution.

REG9B

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Frame End[7:0][2]							

Frame End [7:0]

When this register is read during imaging or navigation, it returns the lower byte of the Frame End Time. The Frame End Time is captured from a free-running timer with 1 us resolution.

REG9C

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Ch Word[31:24][1]/ Coating[1:0][2] , Foundry[3:0][2]							

Ch Word [31:24]
When written, this sets the upper byte of the Challenge Word.

Foundry [3:0]
Used to indicate which foundry was used.
0x00 TSMC
0x01 Patched ROM

REG9D

This register is read only and is unaffected by reset. The value read from this register is 0x17.

D7	D6	D5	D4	D3	D2	D1	D0
Ch Word[23:16][1]/ ChipID [7:0][2]							

Ch Word [23:16]
When written, this sets the second byte of the Challenge Word.

Chip ID [7:0]
These register bits indicate the sensor model in BCD format. The value of 0x17 is used in the Idaho[AES2550] sensor to indicate that this is FPS19.

REG9E

This register is read only and is unaffected by reset. The value read from this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Ch Word[15:8][1] IO_SEL[2]							

Ch Word [15:8]
When written, this sets the third byte of the Challenge Word.

IO_SEL
Indicates the strapping of the IO_SEL pad.
0 USB Interface selected (PSEL=0)
1 Async Serial Interface selected.

REG9F

This register is read only and is unaffected by reset. The value read from this register is dependent on the revision of the sensor.

D7	D6	D5	D4	D3	D2	D1	D0
Ch Word[7:0][1] / Mask Rev [7:0][2]							

Ch Word [7:0]
When written, this sets the lower byte of the Challenge Word.

Mask Rev [7:0]
These register bits are used to allow each revision of the sensor to be identified. The upper 4-bits are used to track major (all mask) revisions while the lower 4-bits are used to track metal only revisions.

Mask Rev [7:4]
0000 A
| |
1111 O
Mask Rev [3:0]
0000 0
| |
1111 15

A value of 0x00 in this register indicates the 'A0' version.

REGA0

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Read Buffered Egain	FSHR Spare [6:0]						

Read Buffered Egain

Controls whether REG8E returns Current Egain or Buffered Egain. For Gnat use only.

0 REG8E Returns Current E-field Gain.

1 REG8E Returns Buffered E-field Gain.

FSHR Spare[6:0]

These register bits go to spare bits in the analog Frame Rate Shift Register.

REGA1

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Sel NCO Clk	-	Excite Test En	Excite Test Data[4:0]				

Sel NCO Clk

Controls the clock to the synthesizer. When using the NCO Clock, this should be enabled at least 100 us prior to imaging.

0 Synthesizer is clocked from 48MHz clock.

1 Synthesizer is clocked from the Numerically Controlled Oscillator (freq control in REGDD-REGDF).

Excite Test En

Controls data to the excitation DAC.

0 Normal Operation. Excitation DAC is driven by the synthesizer.

1 DAC Test. Excitation DAC is controlled by Excite Test Data.

Excite Test Data[4:0]

When Excite Test En is high, this provides settings to the Excitation DAC. The excitation module contains an inverting amplifier so that the lowest code (0x00) results in the highest voltage at the FDRV pin.

REGA2

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
VTERM ON DURING XMIT	BIT CLKON	BIT DCRSTR	ROW DCRSTR	ATE Skip Analog Reset	Limit Drive	Imp Mode	BIT Analog On

VTERM ON DURING XMIT

Controls state of VTERM when sensor is transmitting.

0 Normal Operation. VTERM is Hi-Z when sensor is transmitting.

1 VTERM is always high.

BIT CLKON

Controls gated clocks.

0 Normal Operation. Clocks are gated off when not needed.

1 Clocks remain on.

BIT DCRSTR

Controls DC Restore signal to analog subsystem.

0 Normal Operation. DCRSTR is asserted after each column is enabled and de-asserted to sample.

1 DCRSTR signal is always asserted.

ROW DCRSTR

Controls ROW EN signals to analog subsystem during DC restore intervals.

0 Normal Operation. ROW EN signals are controlled by register bits (REGD6).

1 All ROW EN signals are asserted during DCRSTR.

Limit Drive

Controls the maximum amplitude of the FDRV signal .

0 Normal Operation. No limit on FDRV amplitude.

1 FDRV is limited to 2V p-p to allow reference measurement through analog subsystem operating at 1.8V Vdd.

ATE Skip Analog Reset

Used during ATE test.

0 Normal operation

1 no Analog Reset

IMP Mode

Controls acquisition of Bussed Pixel Data.

0 No Bussed Pixel measurements are made.

1 Bussed Pixel measurements are made every frame.

BIT Analog On

Provides a way to force analog power down signals to remain active.

0 Normal operation. Analog Power down signals are asserted to reduce power.

1 Analog Power Down signals are forced inactive.

REGA3

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
A2DDc_Test[3:0]				Arydc Test[3:0]			

A2DDc_Test [3:0]

These register bits control the state of the A2DDc_Test bits sent to the analog subsystem to select one of the 16 dc levels in the analog channel

0000	VREFP
0001	VCRP
0010	vrcm
0011	VCRN
0100	VREFN
0101	VOFFP
0110	VOFFN
0111	VDDA1 from A2D Bias Generator
1000	VDDA1 from Offset Adjust Block (2X)
1001	VDDA1 from 1st (1X-8X) PGA
1010	VDDA1 from 2nd (1X-8X) PGA
1011	VDDA1 from Level Shifter Block (2X)
1100	VDDA1 from 1st A2D RSD Block
1101	NCO_ION
1110	NCO_VGR
1111	VCM

Arydc_Test [3:0]

These register bits control the state of the Arydc_Test bits sent to the analog subsystem to select one of the 16 dc levels in the pixel array, sense amplifiers, and S/H amplifiers

0000	from A2DDC
0001	vrpix_cds
0010	vrpix_dc
0011	VBP1_CDS (from field 1)
0100	VBP2_CDS (from optical)
0101	VBN2_CDS (from impedance)
0110	VBN1_CDS (from thermal)
0111	OVC_ATST
1000	FD_OFFN
1001	FD_OFFP
1010	VBG_TSD
1011	VPTAT_TSD
1100	VOFFDACN
1101	VOFFDACP
1110	chgpump
1111	EXCIT_VBG

REGA4

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Excite pd	Ary pd	A2d pd	A2Ddig1_en	A2Ddig1_test [3:0]			

Excite pd

This register bit controls the state of the Excite pd bit sent to the analog subsystem. If this bit is asserted the excitation module is powered down as long as BIT Analog On (REGA2) is not asserted.

Ary pd

This register bit controls the state of the Ary pd bit sent to the analog subsystem. If this bit is asserted the array is powered down as long as BIT Analog On (REGA2) is not asserted.

A2d pd

This register bit controls the state of the A2d pd bit sent to the analog subsystem. If this bit is asserted the A/D module is powered down as long as BIT Analog On (REGA2) is not asserted.

A2ddig1 En

Enables the digital test mux to select one of the comparator output bits from each RSD stage in the pipeline ADC (Active High)

A2Ddig1_test [3:0]

Selects one of 16 digital output lines from the pipeline A2D RSD stage. "A2Ddig1_en" must be high or the output will be driven low.

0000	D0_7	1st Stage
0001	D1_7	1st Stage
0010	D0_6	2nd Stage
0011	D1_6	2nd Stage
0100	D0_5	3rd Stage
0101	D1_5	3rd Stage
0110	D0_4	4th Stage
0111	D1_4	4th Stage
1000	D0_3	5th Stage
1001	D1_3	5th Stage
1010	D0_2	6th Stage
1011	D1_2	6th Stage
1100	D0_1	7th Stage
1101	D1_1	7th Stage
1110	D0_0	8th Stage
1111	D1_0	8th Stage

REGA5

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
A2DAc_Test[3:0]				A2DAc_En	A2Ddig2_en	A2Ddig2_test [1:0]	

A2DAc_Test [3:0]

These register bits control the state of the A2DAc_Test bits sent to the analog subsystem.

0000 Diff2Se conversion of selected CDS output
0001 Diff2Se conversion of Offset Adjust Block
0010 Diff2Se conversion of 1st PGA Block
0011 Diff2Se conversion of 2nd PGA Block
0100 Diff2Se conversion of Level Shifter Block
0101 Diff2Se conversion of 1st ADC RSD
0110 Diff2Se conversion of 2nd ADC RSD
0111 Diff2Se conversion of 3rd ADC RSD
1000 Diff2Se conversion of 4th ADC RSD
1001 Diff2Se conversion of 5th ADC RSD
1010 Diff2Se conversion of 6th ADC RSD
1011 Diff2Se conversion of 7th ADC RSD
1100 future
1101 future
1110 future
1111 future

A2DAc_En

This register bit controls the state of the A2DAc_En bit sent to the analog subsystem.

A2Ddig2_en

This register bit controls the state of the A2Ddig2_en bit sent to the analog subsystem.

A2Ddig2_Test [1:0]

These register bits control the state of the A2Ddig2_Test bits sent to the analog subsystem to select one of 4 clock phases used in the clocking of the analog pipeline. A2ddig2_en must be high, or the output will be driven low.

00 PH1_A2D
01 PH1E_A2D
10 PH2_A2D
11 PH2E_A2D

REGA6

This register is reset by Master Reset. The reset value for this register is 0xA6.

D7	D6	D5	D4	D3	D2	D1	D0
FloatN	HIGV [1:0]		FRSR[63:62]			FD LPNAV pd	SWSHR[16]

FloatN

This register bit controls the state of the FloatN bit sent to the analog subsystem.

HiGv [1:0]

This sets the E-field pixel sense amp gain.

00 1x

01 2x

FRSR[63:62]

These are spare bits in the Frame Rate Shift Register (FRSR) that provides controls to the analog subsystem.

FD LPNAV pd

This register bit controls the state of the FD LPNAV pd bit sent to the analog subsystem.

SWSHR[16]

These are spare bits in the Swipe Rate Shift Register (SWSHR) that provides controls to the analog subsystem.

REGA7

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Lvshift	Sense Amp pd	SE Mode	Arydig_en	Arydig_test [3:0]			

Lvshift

This register bit controls the state of the Lvshift bit sent to the analog subsystem.

Lvshift

This register bit controls the state of the Sense Amp pd bit sent to the analog subsystem.

SE Mode

This register bit controls the state of the SE Mode bit sent to the analog subsystem.

Arydig_en

This register bit controls the state of the Arydig_en bit sent to the analog subsystem.

Arydig_test [3:0]

These register bits control the state of the Arydig_test [3:0] bits sent to the analog subsystem to select one of 16 digital output lines associated with pixel array control. "Ary Dig Enable" must be high or the output will be driven low.

0000	GND1
0001	GND1
0010	GND1
0011	GND1
0100	GND1
0101	LED_CTRL
0110	EN_3P3
0111	V2X_Q
1000	EXCIT_Q
1001	START_HISTO
1010	END_HISTO
1011	ARRAY_Q
1100	COL128_Q_RD
1101	GND1
1110	FSHR_Q
1111	A2D_Q

REGA8

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
-	Invert BIT Data	Fixed BIT Data	Dig BIT En	Dig Bit Data [4:0]			

Invert BIT Data

Allows the BIT Data pattern to be inverted.

0 BIT Data is not inverted.

1 BIT Data is inverted.

Fixed BIT Data

Enables a fixed BIT Data pattern using Dig BIT Data. If 8-bit E-field pixel depth is selected, Dig BIT Data (or the compliment if Invert BIT Data is set) is used as the upper nibble of the 8-bit data. The lower nibble is the compliment of the upper nibble.

0 Select pattern from BIT generator.

1 Select Fixed BIT data.

Dig BIT En

Enables Digital BIT. When digital BIT is enabled, the BIT data is substituted for data received from the A/D. Data is captured using the same timing as A/D data.

0 Normal Operation. Imaging data is obtained from the A/D.

1 Imaging data is obtained from BIT source.

Dig BIT Data [4:0]

These bits define BIT data for BIT modes that require it.

The BIT generator produces the following 8-bit data pattern. The BIT generator is reset at the start of each frame.

```
0x57, 0x2B, 0x15, 0x0A, 0x85, 0x42, 0x21, 0x90,
0x48, 0xA4, 0xD2, 0x69, 0x34, 0x9A, 0xCD, 0xE6,
0xF3, 0xF9, 0x7C, 0x3E, 0x1F, 0x8F, 0xC7, 0x63,
0xB1, 0xD8, 0xEC, 0x76, 0xBB, 0x5D, 0xAE,
```

For 4-bit E-field data this results in the following data:

```
0x25, 0x01, 0x48, 0x92, 0xA4, 0x6D, 0x93, 0xEC,
0xFF, 0x37, 0x81, 0x6C, 0xDB, 0x7E, 0x5B, 0x5A,
0x12, 0x80, 0x24, 0x49, 0xDA, 0x36, 0xC9, 0xFE,
0x7F, 0x13, 0xC8, 0xB6, 0xED, 0xB7, 0xA5,
```

REGA9 - REGAB

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Digital Mux N En	Digital Mux N Sel [6:0]						

Digital Mux N Select [6:0]

These bits control the test mux whose output is viewable on GPION if GPION is configured as an output.
REGA9 controls Digital Mux 0 and GPIO0.
REGAA controls Digital Mux 1 and GPIO1.
REGAB controls Digital Mux 2 and GPIO2.

Code	Signal	Code	Signal	Code	Signal
0x80	DCRSTR	0xA0	A2D_DATA[1]	0xC0	TIMER DONE
0x81	COL_CLK	0xA1	A2D_DATA[2]	0xC1	LPO TIMER DONE
0x82	CDS_SIGP	0xA2	A2D_DATA[3]	0xC2	GNAT_READ_ADDR[5]
0x83	CDS_SIGM	0xA3	A2D_DATA[4]	0xC3	GNAT_READ_ADDR[4]
0x84	CDS_SEL_CLK	0xA4	A2D_DATA[5]	0xC4	GNAT_READ_ADDR[3]
0x85	CDS_SEL[0]	0xA5	A2D_DATA[6]	0xC5	GNAT_READ_ADDR[2]
0x86	CDS_SEL[1]	0xA6	A2D_DATA[7]	0xC6	GNAT_READ_ADDR[1]
0x87	CDS_SEL[2]	0xA7	COMP_DATA	0xC7	GNAT_READ_ADDR[0]
0x88	CDS_SEL[3]	0xA8	OSC_IN	0xC8	USB_OE_N
0x89	GND	0xA9	OSC_DISABLE	0xC9	USB_SUSPEND
0x8A	GND	0xAA	APLL_FBCLK	0xCA	USB_RCV
0x8B	GND	0xAB	APLL_PD	0xCB	USB_VP
0x8C	GND	0xAC	APLL_PUB	0xCC	USB_VM
0x8D	GND	0xAD	PLL_DISABLE_N	0xCD	TEST_SIG2[1]
0x8E	GND	0xAE	LPO_IN	0xCE	TEST_SIG2[2]
0x8F	PIXEL_VCM_FLOATN	0xAF	FGR_PRESENT	0xCF	TEST_SIG2[3]
0x90	BUSSED_PIXEL_EN	0xB0	FRAME_SCAN	0xD0	TEST_SIG1[0]
0x91	V2X_CLK	0xB1	EXCITE_ENABLE	0xD1	TEST_SIG1[1]
0x92	SYNTH_DATA[4]	0xB2	FROM_MTC	0xD2	TEST_SIG1[2]
0x93	ANALOG_PD	0xB3	MSTR_RESET	0xD3	TEST_SIG1[3]
0x94	ANALOG_RESET	0xB4	RISC_INT	0xD4	TEST_SIG2[0]
0x95	SWSHR_CLK	0xB5	CLK_DISABLE	0xD5	Inbuf_full
0x96	SWSHR_D	0xB6	DMA1_BUSY	0xD6	Buf_full
0x97	FSHR_CLK	0xB7	DMA2_BUSY	0xD7	Outbuf_full
0x98	FSHR_D	0xB8	LPFD_INTERFERENCE	0xD8	Timer_busy
0x99	SHR_LD	0xB9	LPFD_WAKEUP	0xD9	Lpo_timer_busy
0x9A	FROM_ARYDIG	0xBA	LPFD_FGR_PRESENT	0xDA	Microsec_pulse
0x9B	FROM_A2DDIG1	0xBB	NCO_SER_CODE	0xDB	Excite_window
0x9C	FROM_A2DDIG2	0xBC	NCO_SER_CLK	0xDC	GNAT_READ_ADDR[9]
0x9D	A2D_CLK	0xBD	NCO_SEARCH_DONE	0xDD	GNAT_READ_ADDR[8]
0x9E	A2D_CLK_EN	0xBE	NCO_LOCKED	0xDE	GNAT_READ_ADDR[7]
0x9F	A2D_DATA[0]	0xBF	NCO_CLK_DIV4	0xDF	GNAT_READ_ADDR[6]

REGAC

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Clk Keep On [7:0]							

Clk Keep On [7:0]

These register bits allow forcing individual clock domains to remain on. Implementation details are TBD.

REGAD

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
	ADVrange2V			LPFD Sample Early	LPFD avg[2:0]		

ADVrange2V

This register bit controls the state of the ADVrange2V bit sent to the analog subsystem.

LPFD Sample Early

High places CDS_SIGP in first clock of excitation, low places CDS_SIGP in the second clock of excitation. Reset value is 0.

LPFD avg [2:0]

Specifies the number samples that should be averaged when using Low Power Finger Detect. This may improve results in the presence of interference signals.

000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

REGAE

This register is reset by Master Reset. The reset value for this register is 0x80.

D7	D6	D5	D4	D3	D2	D1	D0
OFFDAC Base[7:0]							

OFFDAC Base[7:0]

This specifies the base value used to set the E-field OFFDAC in the analog subsystem.

REGAF

This register is reset by Power On Reset. The reset value for this register is 0x80.

D7	D6	D5	D4	D3	D2	D1	D0
FD THRESH DAC [7:0]							

FD THRESH DAC[7:0]

This sets the reference voltage to the voltage comparator used for finger detect.

REGB0

This register is reset by Power On Reset. The reset value for this register is 0xFX.

D7	D6	D5	D4	D3	D2	D1	D0
-	GPO Disable [2:0]			-	GPO / GPI [2:0]		

GPO Disable [2:0]

These bits control the direction of the corresponding GPIO pins. A GPIO pin is enabled as an output when the corresponding bit is low.

GPO / GPI [2:0]

When written to these bits specify the state of the GPO signals. The GPO signals are driven to the GPIO pins when the corresponding GPO Enable bit is set. When read these bits indicate the state of the GPIO pins.

REGB1

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Sensor Reset	-	CR1 Sel	CR2 Alt Embw	Analog pd	Analog Reset	ATE Cont. Image	

Sensor Reset

Software emulation of power on reset – use carefully! Typical software use model:

1. Driver detects some type of fatal error or timeout
2. Driver forces a USB Reset
3. Driver sets registry values to indicate a 'cycle port' event occurred.
4. Driver unloads.
5. New driver instance loads.
6. Driver checks registry to see if 'cycle port' event occurred.
7. If cycle port occurred, immediately send a "B1 80" command to reset the sensor.
8. Driver unloads and repeats step 5….

1 Reset sensor – self clearing

CR1 Sel

Controls the algorithm used to generate the Authentication Word.

0 Authentication word is generated using the CR2 algorithm.
1 Authentication word is generated using the CR1 algorithm.

CR2 Alt Embw

Controls which embedded word is used with the CR2 algorithm. This bit is self-resetting and is cleared at the end of each image frame.

0 CR2 uses Embedded Word 1.
1 CR2 uses Embedded Word 2.

Analog pd

Controls the global power down signal to the analog subsystem. BIT Analog On (REGA2) forces the global power down inactive.

0 Power downs to analog modules are controlled by individual power down signals.
1 All analog modules are powered down.

Analog Reset

Controls the Reset signal sent to the analog subsystem. Analog Reset is asserted when Power On Reset or Master Reset is active. It can also be separately controlled through this register.

0 Analog Reset is not asserted.
1 Analog Reset is asserted holding the analog subsystem in the reset state.

ATE Continuous Image

This is used during ATE to put the device in a maximum current mode, in concert with disabling output data in register 0x8F and enabling an image mode in registers 0x80 and x081.

0 Normal Operation.
1 Enables high current condition on the sensor.

REGB2

This register is reset by Master Reset. The reset value for this register is 0x40.

D7	D6	D5	D4	D3	D2	D1	D0
LPO Coarse [1:0]		-	A2D Spare [4:2]			FD OFF D2A SEL	FD HYS EN

LPO Coarse [1:0]

Controls the divider after the Low Power Oscillator (LPO) to determine the clock frequency received by the digital subsystem. Frequencies shown assume that the LPO has been calibrated (see LPO FA in REGD0).

00 LPO Frequency is 320 KHz.
01 LPO frequency is 20 KHz.
10 LPO Frequency is 5 KHz. *When LPO_CA is set to 2 the NextMilliSecCntr is not updated correctly and the MilliSecPulse occurs every other LPO clock (400 us) instead of every ms. The bug is in logic that modifies the counter value when LPO_CA changes, suspend_resume.v Currently LPO_CA is always set to 1 (20 KHz) during Suspend and should not change so there should be no impact from this.*
11 LPO frequency is 1.25 KHz.

A2D Spare [4:2]

These are spare bits for the A/D subsystem.

FD OFF D2A SEL

This controls which DAC is controlling the threshold of the Low Power Finger Detect comparator. This bit is used only when FD HYS EN is low.

0 FD Threshold D/A.
1 OFFDAC.

FD HYS EN

This controls hysteresis on the Low Power Finger Detect comparator.

0 Hysteresis is disabled.
1 Hysteresis is enabled.

REGB3

This register is reset by Power On Reset. The reset value for this register is 0x32.

D7	D6	D5	D4	D3	D2	D1	D0
Startup Dly [7:0]							

Startup Dly [7:0]

This controls the startup delay provided for the analog subsystem. The startup delay is the time between when Analog pd is de-asserted and imaging starts. The actual delay value is (setting + 1) * 1 us.

00000000 1 us
| |
11111111 256 us

REGB4

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	Single CDS En	CDS [3:0]			

Single CDS En

When high this forces the CDS to remain at a single setting when acquiring data. The setting is specified by CDS[3:0]. This bit takes precedence over the Opt Sel and Fngr Drv Sel bits (REGAD).

CDS[3:0]

This specifies the CDS setting to be used when Single CDS En is high. The table below shows CDS selections.

0-7 E-field CDS
8 Impedence Reference
9 TBD
10 TBD

REGB5

This register is reset by Master Reset. The reset value for this register is 0xAB.

D7	D6	D5	D4	D3	D2	D1	D0
Idac[1:0]		Ivrpix [1:0]		Ivrcm[1:0]		Isense amp [1:0]	

Idac [1:0]

Sets the bias current level for all lo-side amplifiers used in the analog channel

00 6.25uA
01 12.5uA
10 25uA
11 50uA

ivrpix [1:0]

Set the bias current level to the amplifier that drives rpix to the RF array

00 12.5uA
01 25uA
10 50uA
11 100uA

Ivrcm [1:0]

Sets the bias current level to the amplifier that drives vrcm to the analog channel

00 12.5uA
01 25uA
10 50uA
11 100uA

Isenseamp [1:0]

Sets the bias current level in the 8-Col-based sense amplifiers

00 2.5uA
01 5uA
10 10uA
11 20uA

REGB6

This register is reset by Master Reset. The reset value for this register is 0x0A.

D7	D6	D5	D4	D3	D2	D1	D0
SHIFT CDS	ALT MULT UPDATED	LIMIT BUF SIZE[1:0]		Ianch [1:0]		Icdsamp [1:0]	

SHIFT CDS

This allows shifting the placement of E-field CDS_SIGP and CDS_SIGM sample pulses.

0 Normal placement of sample pulses. Pulses are launched on internal SYNTH_CLK rising edges.

1 Sample pulses are shifted ½ SYNTH CLK early and launched on SYNTH CLK falling edges.

ALT MULT UPDATED

When this bit is high, UPDATE AT MULT is returned in stead of MULT UPDATED.

LIMIT_BUF_SIZE[1:0]

This limits the number of frames that can be buffered to allow SGC to be more responsive.

00 Allow all of buffer to be used.

01 Only store one frame in buffer.

10 Only store two frames in buffer.

11 Only store three frames in buffer.

Ianch [1:0]

Sets the bias current level in all the fully differential folded-cascade amplifiers, differential to single ended converter amplifiers, and hi-side amplifiers in the differential DACs of the analog channel

00 6.25uA

01 12.5uA

10 25uA

11 50uA

Icdsamp [1:0]

Sets the bias current level in the 8-Col-based sense amplifiers

00 6.25uA

01 12.5uA

10 25uA

11 50uA

REGB7

This register is reset by Master Reset. The reset value for this register is 0x80.

D7	D6	D5	D4	D3	D2	D1	D0
SA8_TMB	V2X_SPARE2						LOAD SR

SA8_TMB

When low this bit reconfigures the input to the BPR CDS to be from the last E-field sense amp.

V2X_SPARE2

This is a spare bit in the Swipe Rate Shift Register (SHSHR) that provides controls to the analog subsystem.

Load SR

When written with a 1 the load signal to the analog subsystem will be set active. This causes the analog subsystem control output registers to be updated from the shift register contents. This bit is self resetting.

REGB8

This register is reset by Master Reset. The reset value for this register is 0x40.

D7	D6	D5	D4	D3	D2	D1	D0
-	FNGRDrvBias [2:0]			MTC SEL[1:0]		FRSR [32:31]	

FNGRDrvBias [2:0]

These register bits control the state of the FNGRDrvBias [2:0] bits sent to the analog subsystem.

MTC Sel [1:0]

Selects Macro Test Chain output.

00 Bypass Mode
01 Select chain of 20 ND2 gates
10 Select chain of 20 NR2 gates
11 Select chain of 10 FA1 gates

FRSR [32:31]

Controls the state of Frame Rate Shift Register bits 32-31.

REGB9

This register is reset by Power On Reset. The reset value for this register is 0x24.

D7	D6	D5	D4	D3	D2	D1	D0
PLL On Delay [3:0] [2]				Osc On Delay [3:0] [2]			

PLL On Delay [3:0]

These bits specify the amount of time that the sensor should wait between enabling the PLL and enabling clocks to the digital logic. The delay is specified in units of LPO CLK when LPO_CA is set to 01b. This corresponds to a resolution of 50 us (+/- 10%) when the LPO has been calibrated. For other LPO_CA settings the bits are used as required to maintain a 50 us resolution. Non zero settings will always result in a minimum delay of one LPO clock at the programmed LPO_CA setting. A setting of 0 is valid and will result in no delay (this could be used with an external 48MHz clock).

Osc On Delay [3:0]

These bits specify the amount of time that the sensor should wait between enabling the Oscillator and enabling the PLL. The delay is specified in units of 4xLPO CLK when LPO_CA is set to 01b. This corresponds to a resolution of 200 us (+/- 10%) when the LPO has been calibrated. For other LPO_CA settings the bits are used as required to maintain a 200 us resolution. Non zero settings will always result in a minimum delay of one LPO clock at the programmed LPO_CA setting. A setting of 0 is valid and will result in no delay (this could be used with an external clock).

REGBA

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
SHSHR[14]	-	BPR HIGV[1:0]		Buffer Flush		SEND FRSR	SEND SWSHR

SWSHR[14]
These are spare bits in the Swipe Rate Shift Register (SWSHR) that provides controls to the analog subsystem.

BPR HIGV[1:0]
These control the state of the BPR HIGV bits in the analog subsystem. Note that this was a hardware change effective with A1 silicon.

Buffer Flush
When written with a 1 any data in internal buffers will be made available to the active interface. This bit is self resetting.

Send FRSR
When written with a 1 the Frame Rate Shift Register will be sent to the analog subsystem. This bit is self resetting.

Send SWSHR
When written with a 1 the Swipe Rate Shift Register will be sent to the analog subsystem. This bit is self resetting.

REGBB

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
-	Analog Test Mode	Analog TM [5:0]					

Analog Test Mode
This bit controls the reference voltage to the DIFF2SE amplifier in the analog subsystem.
0 Normal Operation. DIFF2SE amplifier receives Vrpix CDS.
1 CDS Test Mode active. DIFF2SE amplifier receives Vrpix DC.

Analog TM [5:0]
These bits control test modes in the analog subsystem.

REGBC

This register is reset by Master Reset. The reset value for this register is 0x04.

D7	D6	D5	D4	D3	D2	D1	D0
A2D Clk Sel [1:0]		Excite Spare [2]	COPY HIGV[1:0]		A2D BGtrim [2:0]		

A2D Clk Sel [1:0]

Specifies the frequency of the A/D clock.

00 12 MHz
01 6 MHz
10 3 MHz
11 1.5 MHz

Excite Spare [2]

These are spare bits for the Excitation module.

COPY HIGV [1:0]

This bits are used for the HIGV setting when USE BPR REG is high. They are not mapped to the BPR HIGV controls and should be set to match the E-field HIGV setting.

A2D BGtrim [2:0]

These register bits control the state of the A2D BGtrim [2:0] bits sent to the analog subsystem.

REGBD

This register is reset by Master Reset. The reset value for this register is 0x13.

D7	D6	D5	D4	D3	D2	D1	D0
LPO IN [15:8]							

REGBE

This register is reset by Master Reset. The reset value for this register is 0x88.

D7	D6	D5	D4	D3	D2	D1	D0
LPO IN [7:0]							

LPO IN [15:0]

This specifies the lower byte of an LPO time value. For LPO Calibration, this specifies the number of LPO cycles used for calibration. For Low Power Finger Detect, this specifies the delay between detect cycles with a fixed resolution of 0.8 ms. In this mode only the lower order 11 bits are used sto specify the delay. For Image Based Finger Detect, this specifies the delay between detect cycles in number of LPO clocks. The time that this corresponds to is dependent on the LPO Coarse setting (REGB2) and LPO calibration (using LPO Freq Adjust in REGD0).

REGBF

This register is reset by Master Reset. The reset value for this register is 0x10.

D7	D6	D5	D4	D3	D2	D1	D0
		Quadrature Mode	Noise Floor Mode	RSR DIR [1:0]		RSR LEVEL [1:0]	

Quadrature Mode
Enables obtaining quadrature image data.
0 Normal Operation
1 Use quadrature imaging (sine-wave, 8-bit, 64-col)

Noise Floor Mode
Enables obtaining noise floor measurement data from the sensor.
0 Normal Operation
1 Collect noise floor data. Number of image frames specified by N-shot is returned in continuous imaging mode. N-1 frames have Finger Detect true, the last has Continuous Done true and Finger Detect false.

RSR DIR [1:0]
00 Enable detecting down motion.
01 Enable detecting up motion.
10 Enable detecting both up and down motion.
11 Reserved.

RSR LEVEL [1:0]
00 Disabled. All image slices are returned.
01 Leading RSR. Slices before first motion is detected are discarded.
10 Simple RSR. All slices without motion are discarded.
11 Super RSR. Slices with 0-3 pixels of Y motion are discarded.

The size of the internal buffer areas used with RSR require that the frame message length be less than 1K in size. If 8-bit data is selected, this requires the number of columns scanned to be <= 64. If a wider scan area is selected the Gnat will disable RSR.

REGC0

This register is reset by Master Reset. The reset value for this register is 0x0D.

D7	D6	D5	D4	D3	D2	D1	D0
BP Excite Cycle[2:0]			BP Init Freq[4:0]				

BP Excite Cycle [2:0]
These register bits control the number of excitation cycles used when in Bussed Pixel mode.

BP Init Freq [4:0]
These register bits control the initial excitation frequency when in Bussed Pixel mode.

REGC1

This register is reset by Master Reset. The reset value for this register is 0x08.

D7	D6	D5	D4	D3	D2	D1	D0
BP Phase Step[7:0]							

BP Phase Step [7:0]
These register bits control the phase step used when Interleaved Bussed Pixel mode is enabled.

REGC2

This register is reset by Master Reset. The reset value for this register is 0x92.

D7	D6	D5	D4	D3	D2	D1	D0
BP Pixel Avg[2:0]			BP Gain Inc[1:0]		VCM DCRSTR	VCM State	Bussed Pixel Enable

BP Pixel Avg [2:0]
These register bits control pixel averaging when in Bussed Pixel mode.

BP Gain Inc [1:0]
These register bits control the gain increment used when Interleaved Bussed Pixel mode is enabled.

VCM DCRSTR
When this bit is high the PIXEL_VCM_FLOATN signal to the analog subsystem is driven with DCRSTR. When this bit is low PIXEL_VCM_FLOATN is driven to the level specified by VCM State.

VCM State
This register bit controls the state of the PIXEL_VCM_FLOATN signal to the analog subsystem when VCM DCRSTR is low.

Bussed Pixel En
This register bit controls the state of the BUSSED PIXEL EN signal sent to the analog subsystem.

REGC3

This register is reset by Master Reset. The reset value for this register is 0x08.

D7	D6	D5	D4	D3	D2	D1	D0
BP Phase Init[7:0]							

BP Phase Init [7:0]
These register bits control sample phase when in Bussed Pixel mode.

REGC4

This register is reset by Master Reset. The reset value for this register is 0xDF.

D7	D6	D5	D4	D3	D2	D1	D0
BP Freq Start[3:0]				BP Freq Stop[3:0]			

BP Freq Start [3:0]
These register bits control the starting frequency when Interleaved Bussed Pixel mode is enabled.

BP Freq Stop [3:0]
These register bits control the stoping frequency when Interleaved Bussed Pixel mode is enabled.

REGC5

This register is reset by Master Reset. The reset value for this register is 0xF2.

D7	D6	D5	D4	D3	D2	D1	D0
BP Gain[3:0]				Fixed BP Gain	BPR Excite Drive [2:0]		

BP Gain [3:0]

These register bits provide the system gain setting when in Bussed Pixel mode and measuring the Bussed Pixel plate. The BP Gain table is shown below.

	Drive	HiGv	Gain1	Gain2	Gain3	Total
0000	1/8	1x	1x	1x	1x	1/8
0001	1/4	1x	1x	1x	1x	1/4
0010	1	1x	1x	1x	1x	1
0011	1	1x	1x	1x	2x	2
0100	1	1x	2x	1x	2x	4
0101	1	1x	2x	2x	2x	8
0110	1	1x	4x	2x	2x	16
0111	1	1x	4x	4x	2x	32
1000	1	1x	8x	4x	2x	64
1001	1	1x	8x	8x	2x	128
1010	1	1x	16x	8x	2x	256
1011	1	1x	16x	16x	2x	512
1100	1	1x	16x	16x	4x	1024
1101	1	2x	16x	16x	4x	2048
1110	1	2x	16x	16x	4x	2048
1111	1	2x	16x	16x	4x	2048

Fixed BP Gain

When this bit is set, no gain adjustments are made in Bussed Pixel mode.

BP Excite Drive [3:0]

These bits specify the Excite Drive level used in Bussed Pixel mode.

REGC6

This register is reset by Master Reset. The reset value for this register is 0xB0.

D7	D6	D5	D4	D3	D2	D1	D0
BP Phase Stop[7:0]							

BP Phase Stop [7:0]

These register bits control the stopping phase when Interleaved Bussed Pixel mode is enabled.

REGC7

This register is reset by Master Reset. The reset value for this register is 0xB8.

D7	D6	D5	D4	D3	D2	D1	D0
BP Phase Loop Pnt[7:0]							

BP Phase Loop Pnt [7:0]

These register bits control the phase looping point when Interleaved Bussed Pixel mode is enabled.

REGC8

This register is reset by Master Reset. The reset value for this register is 0x50.

D7	D6	D5	D4	D3	D2	D1	D0
BP Phase Loop Val[7:0]							

BP Phase Loop Val [7:0]

These register bits control the phase looping value when Interleaved Bussed Pixel mode is enabled.

REGC9

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
BP Offdac[7:0]							

BP Offdac [7:0]

These register bits control the Offset DAC when Bussed Pixel mode is enabled.

REGCA

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
FRSR[57:56][20:15]							

FRSR[57:56][20:15]
These are spare bits in the Frame Rate Shift Register (FRSR) that provides controls to the analog subsystem.

REGCB

This register is reset by Master Reset. The reset value for this register is 0x02.

D7	D6	D5	D4	D3	D2	D1	D0
BPRGAIN3 [1:0]		BPRGAIN2 [2:0]			BPRGAIN1 [2:0]		

BPRGAIN3 [1:0]
Specifies the gain setting for the Offset Adjust and Level Shift amplifiers.
00 1X
01 2X
10 4X
11 4X

BPRGAIN2 [2:0]
Specifies the gain setting for the Second PGA.
000 1X
001 2X
010 4X
011 8X
100 16X
101 16X
110 16X
111 16X

BPRGAIN1 [2:0]
Specifies the gain setting for the First PGA.
000 1X
001 2X
010 4X
011 8X
100 16X
101 16X
110 16X
111 16X

REGCC

This register is reset by Master Reset. The reset value for this register is 0x80.

D7	D6	D5	D4	D3	D2	D1	D0
FRSR[54][44:38]							

FRSR[54][44:38]
These are spare bits in the Frame Rate Shift Register (FRSR) that provides controls to the analog subsystem.

REGCD

This register is reset by Master Reset. The reset value for this register is 0x80.

D7	D6	D5	D4	D3	D2	D1	D0
BPR Offdac[7:0]							

BPR Offdac [7:0]

This specifies the OFFDAC to be used when by the analog subsystem when making a bussed pixel reference measurement.

REGCE

This register is reset by Master Reset. The reset value for this register is 0x03.

D7	D6	D5	D4	D3	D2	D1	D0
		USE BPR REG	USE BP REG		BP FDRV BIAS[2:0]		

USE BPR REG

When this is high the BPR registers are sent to the analog subsystem instead of the E-field settings.

USE BP REG

When this is high the BP registers are sent to the analog subsystem instead of the E-field settings.

REGC5 must be written to force a gain setting decode update after enabling USE BP REG. REG8E must be written to force a gain decode update after disabling USE BP REG.

BP FDRV BIAS [2:0]

These register bits control the state of the FNGRDrvBias [2:0] bits sent to the analog subsystem when Bussed Pixel registers are enabled.

REGCF

This register is reset by Master Reset. The reset value for this register is 0x04.

D7	D6	D5	D4	D3	D2	D1	D0
			SEL_1P5_CYCLES	EXCITE_DLY[3:0]			

SEL_1P5_CYCLES
When high selects 1 ½ cycle excitation, low selects 1 cycle excitation. Reset value is low.

EXCITE_CLY[3:0]
Sets the delay from DC Restore falling edge to the start of excitation in units of SYNTH_CLK. The reset value is 4.

REGD0

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
CDS Test Mode			LPO Freq Adjust[4:0]				

CDS Test Mode
When high the CDS is placed in a test mode by holding CDS_SIGP at the constant level specified by SIGP State (REGCF) and CDS_SIGM at the opposite level.

LPO Freq Adjust[4:0]
This allows adjusting the frequency of the LPO to improve accuracy.

REGD1

This register is reset by Master Reset. The reset value for this register is 0x40.

D7	D6	D5	D4	D3	D2	D1	D0
	BPR PD			Row Offset Disable	-	V2X Clk Sel [1:0]	

BPR PD
When this bit is high the BPR REF CDS has power down asserted.

Row Offset Disable
When this bit is set the E-field Row Offset values (REGD2-REGD5) are not added to the E-field Base Offdac setting. Each row receives the E-field Base Offdac value unmodified.

V2X Clk Sel [1:0]
This selects frequency of the clock driven to the analog subsystem voltage doubler.
00 off (VDCLK is set low)
01 375 KHz
10 750 KHz
11 1.5 MHz

REGD2

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Row 0 Offset [3:0]				Row 1 Offset [3:0]			

Row 0 Offset[3:0]
This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 0. This allows compensating for row related offsets. A value of 0111b specifies an offset of 7 and a value of 1001b specifies an offset of -7.

Row 1 Offset[3:0]
This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 1. This allows compensating for row related offsets.

REGD3

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Row 2 Offset [3:0]				Row 3 Offset [3:0]			

Row 2 Offset[3:0]
This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 2. This allows compensating for row related offsets.

Row 3 Offset[3:0]
This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 3. This allows compensating for row related offsets.

REGD4

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Row 4 Offset [3:0]				Row 5 Offset [3:0]			

Row 4 Offset[3:0]
This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 4. This allows compensating for row related offsets.

Row 5 Offset[3:0]
This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 5. This allows compensating for row related offsets.

REGD5

This register is reset by Power On Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
Row 6 Offset [3:0]				Row 7 Offset [3:0]			

Row 6 Offset[3:0]

This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 6. This allows compensating for row related offsets.

Row 7 Offset[3:0]

This is a signed 4-bit value that specifies the value that should be added (or subtracted) from the OFFDAC Base value when imaging Row 7. This allows compensating for row related offsets.

REGD6

This register is reset by Master Reset. The reset value for this register is 0xFF.

D7	D6	D5	D4	D3	D2	D1	D0
Row En[7:0]							

Row En [7:0]

This field controls switches in series with the DCRSTR switch for each pixel row. When not using Bussed Pixel Mode this register should be set to 0xFF. In Bussed Pixel Mode, bits set to 0 will exclude the corresponding row from the bussed pixel plate. Row 0 is the upper row in the array with ball A1 in the upper left corner.

REGD7

This register is reset by Master Reset. The reset value for this register is 0x20.

D7	D6	D5	D4	D3	D2	D1	D0
MAX PD INT [7:0]							

MAX PD INT [7:0]

This specifies the integer portion of the synthesizer maximum Phase Delta (PD). This is the value used by the synthesizer to add to the accumulator at each clock when Excite Freq is set to select the highest frequency.

The desired value can be determined by $MAXPD = \frac{256}{\left(\frac{f_{clk}}{f_{synth}}\right)}$ where f_{clk} is the synthesizer clock frequency (typically 48 MHz when the sensor is not using the NCO clock for the synthesizer) and f_{clk} is the desired synthesizer output frequency when Excite Freq is set to select the highest frequency.

REGD8

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
MAX PD FRAC [15:8]							

MAX PD FRAC [15:8]

This specifies the upper byte of the fractional portion of the synthesizer maximum Phase Delta (MAX PD). This is the value used by the synthesizer to add to the accumulator at each clock when Excite Freq is set to select the highest frequency.

REGD9

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
MAX PD FRAC [7:0]							

MAX PD FRAC [7:0]

This specifies the lower byte of the fractional portion of the synthesizer maximum Phase Delta (MAX PD). This is the value used by the synthesizer to add to the accumulator at each clock when Excite Freq is set to select the highest frequency.

REGDA

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
		BP HiGv[1:0]			BP Excite Drive[2:0]		

BP HiGv [1:0]

This sets the E-field pixel sense amp gain when Use BP Reg (REGCE[4]) is high. The Gnat uses these registers to decode BP Gain setting.

00 1x
01 2x

BP Excite Drive [2:0]

This sets peak drive level for the excitation signal in sine mode when Use BP Reg (REGCE[4]) is high. The Gnat uses these registers to decode BP Gain setting.

000 1/32 * V2XOUT * 0.9
001 1/16 * V2XOUT * 0.9
010 1/8 * V2XOUT * 0.9
011 ¼ * V2XOUT * 0.9
100 ½ * V2XOUT * 0.9
101 V2XOUT * 0.9
110 V2XOUT * 0.9
111 V2XOUT * 0.9

REGDB

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
BPGAIN3[1:0]		BPGAIN2[2:0]			BPGAIN1[2:0]		

BPGAIN3 [1:0]

Specifies the gain setting for the Offset Adjust and Level Shift amplifiers when Use BP Reg (REGCE[4]) is high. The Gnat uses these registers to decode BP Gain setting.

00 1X
01 2X
10 4X
11 4X

BPGAIN2 [2:0]

Specifies the gain setting for the Second PGA when Use BP Reg (REGCE[4]) is high. The Gnat uses these registers to decode BP Gain setting.

000 1X
001 2X
010 4X
011 8X
100 16X
101 16X
110 16X
111 16X

BPGAIN1 [2:0]

Specifies the gain setting for the First PGA when Use BP Reg (REGCE[4]) is high. The Gnat uses these registers to decode BP Gain setting.

000 1X
001 2X
010 4X
011 8X
100 16X
101 16X
110 16X
111 16X

REGDC

This register is reset by Master Reset. The reset value for this register is 0x07.

D7	D6	D5	D4	D3	D2	D1	D0
DEBUG CTRL2 [4:0]					BP Num Ref Sweeps [2:0]		

DEBUG CTRL2 [4:0]

These bits are used to enable various debug features included in the firmware.

BIT	FUNCTION
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Enable Impedence Debug Messages

BP Num Ref Sweeps [2:0]

This specifies the number of frequency and phase sweeps of interleaved Bussed Pixel measurements that will include Reference data.

000	No sweeps include reference data
001	First complete sweep of Init Freq -> End Freq will include reference data
010	First two complete sweeps of Init Freq -> End Freq will include reference data
011	First three complete sweeps of Init Freq -> End Freq will include reference data
100	First four complete sweeps of Init Freq -> End Freq will include reference data
101	First five complete sweeps of Init Freq -> End Freq will include reference data
110	First six complete sweeps of Init Freq -> End Freq will include reference data
111	First seven complete sweeps of Init Freq -> End Freq will include reference data

REGDD

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
DEBUG CTRL1 [7:0]							

DEBUG CTRL1 [7:0]

These bits are used to enable various debug features included in the firmware.

BIT	FUNCTION
7	Enable Extended Phase Sweep Messages
6	Enable Finger Detect and Noise Detect debug messages
5	Use NGC instead of HGC
4	Disable Histogram Correction
3	HGC – Limit MULT/OFFSET; NGC – Enable compensation
2	HGC Debug – deliver all images
1	Disable HGC/NGC Init
0	Enable Run Cal Debug

REGDE

This register is reset by Master Reset. The reset value for this register is 0x10.

D7	D6	D5	D4	D3	D2	D1	D0
SYNTH NCO TM			NCO CLK CNT [12:8]				

SYNTH NCO TM [2:0]

Controls test modes implemented in the synthesizer NCO control module.

000 Normal Operation
001 Set mid frequency (code = 10'd512)
010 Set highest frequency (code = 10'd1023)
011 Set lowest frequency (code = 10'd0)
100 Disable adjustments, stay at current code
101 Increment code when SYNTH NCO TM goes from 100b to 101b
110 Decrement code when SYNTH NCO TM goes from 100b to 110b
111 Reserved

NCO CLK CNT [12:8]

These are the upper bits of a control word that specifies the frequency of the Numerically Controlled Oscillator (NCO) used to provide an alternate clock to the synthesizer module. The remaining bits for this are in REGDF. The alternate clock is enabled by setting SEL NCO CLK (REGA1).

The programmed value is calculated by $NCO\_CLK\_CNT = \frac{f_{synth\_clk}}{f_{system\_clk}} \cdot 4096$

where f_{synth_clk} is the desired clock frequency to the synthesizer and f_{system_clk} is the sensor internal clock frequency (typically 48 MHz). The result should be rounded to the nearest integer value.

REGDF

This register is reset by Master Reset. The reset value for this register is 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
NCO CLK CNT [7:0]							

NCO CLK CNT [7:0]

These are the lower bits of a control word that specifies the frequency of the Numerically Controlled Oscillator (NCO) used to provide an alternate clock to the synthesizer module.

Appendix B – USB Interface Descriptors

The tables below show the Device, Configuration, Interface, and String Descriptor values provided by the Idaho[AES2550] sensor.

Field	Index	Value	Meaning
bLength	0	0x12	Length of this descriptor = 18 bytes
bDescriptorType	1	0x01	Descriptor Type = Device
bcdUSB(L)	2	0x00	USB spec. version 2.00 (L)
bcdUSB(H)	3	0x02	USB spec. version 2.00 (H)
bDeviceClass	4	0xFF	Device class (FF is vendor specific)
bDeviceSubClass	5	0xFF	Device sub-class (FF is vendor specific)
bDeviceProtocol	6	0xFF	Device Protocol (FF is vendor specific)
bMaxPacketSize0	7	0x08	Max Packet size for EP0 = 8 bytes
idVendor(L)	8	0xFF	Vendor ID (L)
idVendor(H)	9	0x08	Vendor ID (H)
idProduct(L)	10	0x50	Product ID low byte
idProduct(H)	11	0x25	Product ID high byte
bcdDevice(L)	12	Mask Rev	Device ID (L)
bcdDevice(H)	13	0x19	Device ID (H)
iManufacturer	14	0x00	None
iProduct	15	0x01	Product String – “Fingerprint Sensor”
iSerialNumber	16	0x00	None
bNumConfigurations	17	0x01	One configuration in this interface

Table 17 Device Descriptor

Field	Index	Value	Meaning
bLength	0	09h	Length of this descriptor = 9 bytes
bDescriptorType	1	02h	Type = Configuration
wTotalLength(L)	2	20h	Total Length(L) including Interface and Endpoint descriptors
wTotalLength(H)	3	00h	
bNumInterfaces	4	01h	Number of interfaces in this configuration
bConfigurationValue	5	01h	Configuration value used by ‘Set Configuration’ to select this interface
iConfiguration	6	00h	00h = no string reference
bmAttributes	7	A0h	A0h, Attributes: bus-powered, remote wake-up supported
MaxPower	8	32h	Max current =100mA

Table 18 Default Configuration Descriptor

Field	Index	Value	Meaning
bLength	0	09h	Length of the Interface descriptor = 9 bytes
bDescriptorType	1	04h	Descriptor type = interface
bInterfaceNumber	2	00h	Zero based index of this interface = 0
bAlternateSetting	3	00h	Alternate setting =0
bNumEndpoints	4	02h	Number of endpoints in this interface (not counting endpoint0)
bInterfaceClass	5	FFh	Interface Class = vendor specific
bInterfaceSubClass	6	FFh	Interface Sub Class = vendor specific
bInterfaceProtocol	7	FFh	Interface Protocol = vendor specific
iInterface	8	00h	Index to string descriptor = none

Table 19 Default Interface 0, Alternate Setting 0 Descriptor

Field	Index	Value	Meaning
bLength	0	07h	Descriptor length = 7 bytes long
bDescriptorType	1	05h	ENDPOINT descriptor
bEndpointAddress	2	81h	In endpoint, endpoint #1
bmAttributes	3	02	xfr type = Bulk
wMaxPacketSize(L)	4	40h	Max Packet Size = 64 bytes
wMaxPacketSize(H)	5	00h	
bInterval	6	00h	Polling interval in milliseconds
Field		Value	Meaning
bLength	0	07h	Descriptor length = 7 bytes long
bDescriptorType	1	05h	ENDPOINT descriptor
bEndpointAddress	2	02h	Out endpoint, endpoint #2
bmAttributes	3	02h	xfr type = Bulk
wMaxPacketSize(L)	4	10h	Max Packet Size = 16 bytes
wMaxPacketSize(H)	5	00h	
bInterval	6	00h	Polling interval in milliseconds

Table 20 Default Interface 0, Alternate Setting 0, Bulk Endpoint Descriptors

Field	Index	Value	Meaning
bLength	0	04h	String Index 0
bDescriptorType	1	03h	String descriptor type
wLANGID(0)(L)	2	09h	Language ID for English (L)
wLANGID(1)(H)	3	04h	Language ID for English (H)

Table 21 String 0 Descriptor

Field	Index	Value	Meaning
bLength	0	26h	String Index 1
bDescriptorType	1	03h	String descriptor type
bString	2	4600h	“Fingerprint Sensor” – in UNICODE format “F”
	4	6900h	“i”, 00
	6	6E00h	“n”, 00
	8	6700h	“g”, 00
	10	6500h	“e”, 00
	12	7200h	“r”, 00
	14	7000h	“p”, 00
	16	7200h	“r”, 00
	18	6900h	“i”, 00
	20	6E00h	“n”, 00
	22	7400h	“t”, 00
	24	2000h	“ “, 00
	26	5300h	“S”, 00
	28	6500h	“e”, 00
	30	6E00h	“n”, 00
	32	7300h	“s”, 00
	34	6F00h	“o”, 00
	36	7200h	“r”, 00

Table 22 String 1 Descriptor

Appendix C – Internals

Internal design details are contained in the linked appendix here:

AES2550_Internals_V0.1.doc